PRACTICAL

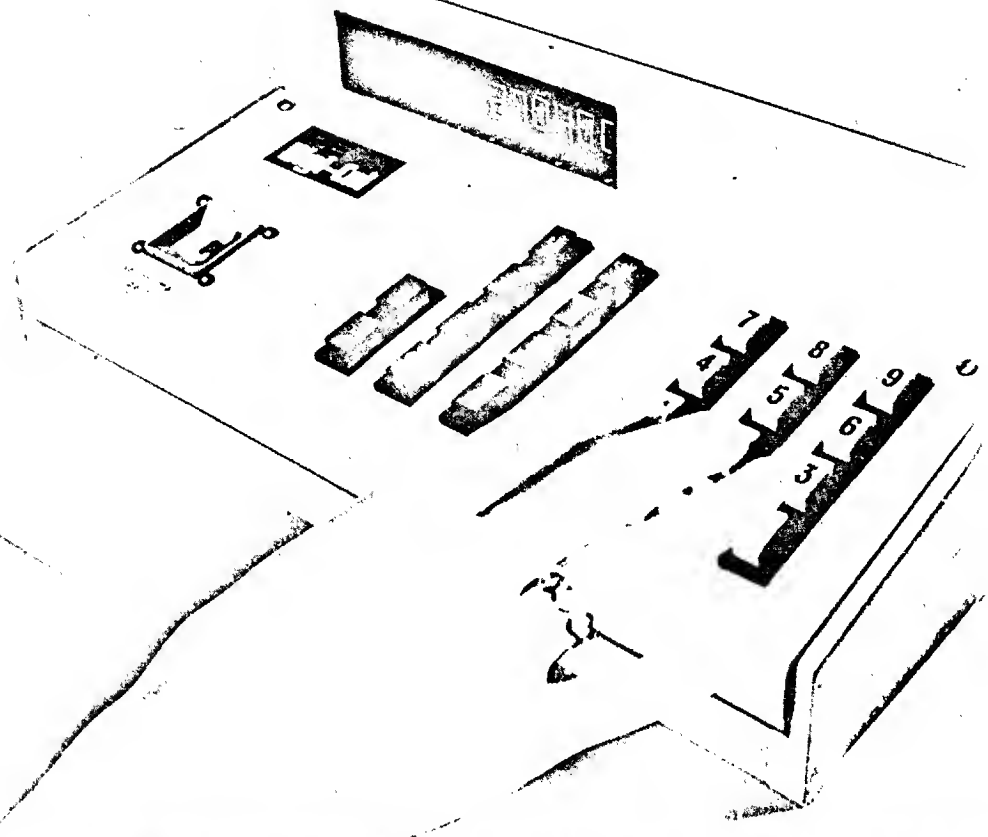
ELECTRONICS

JULY 1972

20p

AT LAST!

ADDS....
SUBTRACTS....
MULTIPLIES....
DIVIDES....
AUTOMATICALLY SQUARES....
and OPERATES WITH STORED CONSTANT



PE

BY R.W.COLES

WE HAVE all become familiar with the host of mechanically operated calculating machines, typified by the supermarket cash-register, which have been with us for many years. The ingenious mechanisms used in these machines can even be coaxed to perform multiplication or division in a simple way, but they are not up to the standard required for general mathematical problems, and have never made much of an inroad into this sphere, where the slide-rule has reigned supreme until very recently.

With the advent of the digital computer employing transistors, and later, integrated circuits, it was soon recognised that it would be possible to build small computers on the lines of mechanical calculators, which would give much simpler operation and a more versatile problem solving capability.

We are now witnessing the heyday of the offspring of the computer/mechanical calculator marriage, and the numbers of small electronic problem solvers becoming available is increasing dramatically every year, bringing big-system electronics to many desk corners.

AMATEUR CONSTRUCTORS

Up to now there has not been an electronic calculator design suitable for amateur constructors, despite the availability of all the necessary integrated circuits. This is mainly due to the fact that the know-how accumulated by the manufacturers of commercial calculators is very jealously guarded, and, to the uninitiated, calculator circuitry does seem quite complex.

Digi-Cal sets out to redress this situation, being designed specifically for home construction and simplified as far as possible without sacrifice of performance. Digi-Cal is a fast flexible tool for performing calculations required in the home, school or laboratory. It can be built using basic techniques and requires no access to expensive test equipment such as oscilloscopes. The prototype was built entirely on the kitchen table!

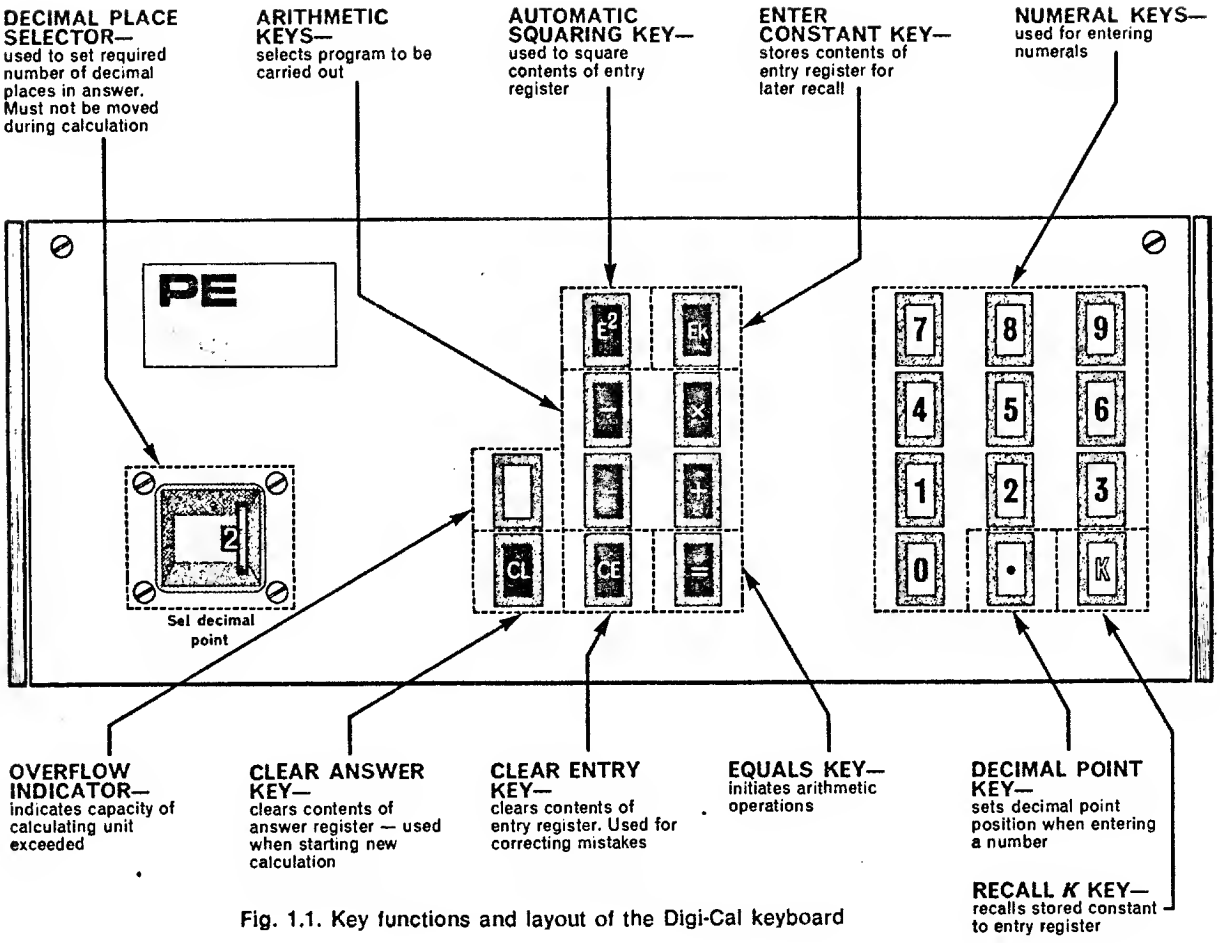


Fig. 1.1. Key functions and layout of the Digi-Cal keyboard

The basic Digi-Cal design has been intended from the outset to be as open-ended as possible to allow for extra features and constructor options. The arithmetic programmes are all easily altered by simply wiring in extra diodes, the constant store and the auto-squaring facility may be omitted and included at a later date, or even omitted altogether, and there are many possible performance improvements for which the design allows without major reconstruction.

All the logic is built on removable cards for easy access, and the complete calculator is housed in a modified "Contil" Mod-2 case with a matching keyboard, making Digi-Cal easily portable.

USING DIGI-CAL

The manipulation of numbers and the initiation of an arithmetic process is carried out using the keyboard, a vital part of any calculator and one which must be carefully thought out both mechanically and electronically. The keyboard is shown in Fig 1.1.

Entries are made by pressing figure keys in the correct sequence, interposing the decimal point where required if necessary. When the first figure key is pressed the display automatically switches from the last anwer to display the new entry, the old answer remaining in store. As subsequent figure keys are pressed they enter from the right taking the decimal point with them, in its correct position, as soon as it is entered. See Figure Entry.

The actual number of figures after the decimal point is immaterial at this point since Digi-Cal positions the numbers automatically before starting a calculation. However, if too many figures are entered, the entry register locks to prevent any further figure inputs, so that if the keyboard is set to give answers to three places, after three places of decimals no further figures can enter the calculator.

With a number entered in the entry register the next step is to select the arithmetic function required, and this is achieved by pressing the appropriate black key. The function entered will remain valid for all subsequent calculations until a different function is required and another key pressed. This means that a whole series of numbers may be added, for example, with only one depression of the add.(+) key. Each time a new number is entered the equals key is pressed and the number is automatically added to the previous total.

Pressing the equals key starts the calculation, and when the programme for that function is complete the display switches to the answer register to display the result.

All operations are performed on the previous answer, so when starting with an empty answer register (after it has been cleared by the clear key) the first number entered must be added into it before the calculation proper begins. If a mistake is made when entering figures, the entry register can be cleared with the clear entry (CE) key.

- ENTRIES UP TO SIX DIGITS WITH FLOATING DECIMAL POINT CAN BE MADE, ANSWERS ARE PRODUCED UP TO EIGHT DIGITS LONG WITH THE DECIMAL POINT IN ONE OF FOUR PRESELECTED POSITIONS

- ENTRIES AND ANSWERS ARE DISPLAYED ON EIGHT SEVEN-SEGMENT INDICATORS WITH AN ADVANCED LEADING-EDGE ZERO-SUPPRESSION SYSTEM

- SIMPLE TO USE, PROBLEMS CAN BE ENTERED AS THEY WOULD BE WRITTEN DOWN

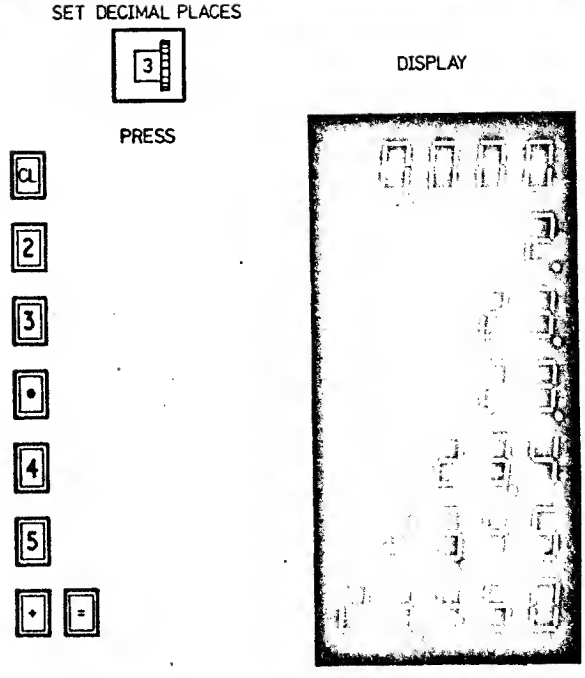
- EMPLOYS READILY AVAILABLE TTL INTEGRATED CIRCUITS THROUGHOUT

OPERATIONS USING A CONSTANT

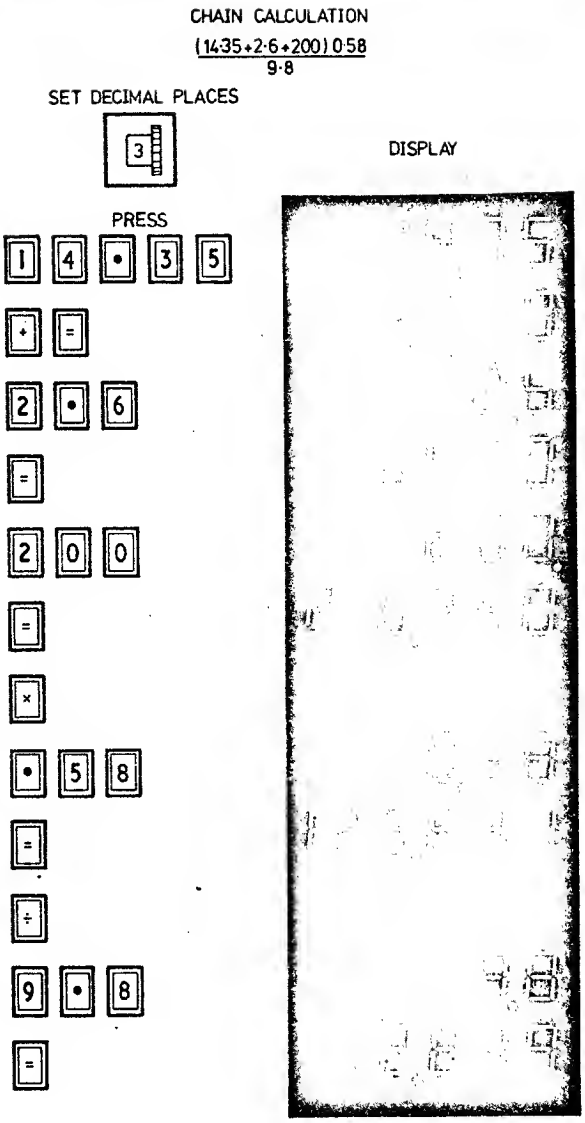
When operation with a constant is required the constant is entered in the entry register in the normal way, except that it must be positioned with the decimal point in the proper place, and then the EK key is pressed to store the constant for future use. When the constant is required the white K key is pressed, which instantly recalls the stored number to the entry register ready for use. The constant remains in store until replaced or the machine switched off.

The following examples will show just how simple Digi-Cal is to use and how useful it can be to solve a wide range of problems encountered in all walks of life.

FIGURE ENTRY



EXAMPLE ONE

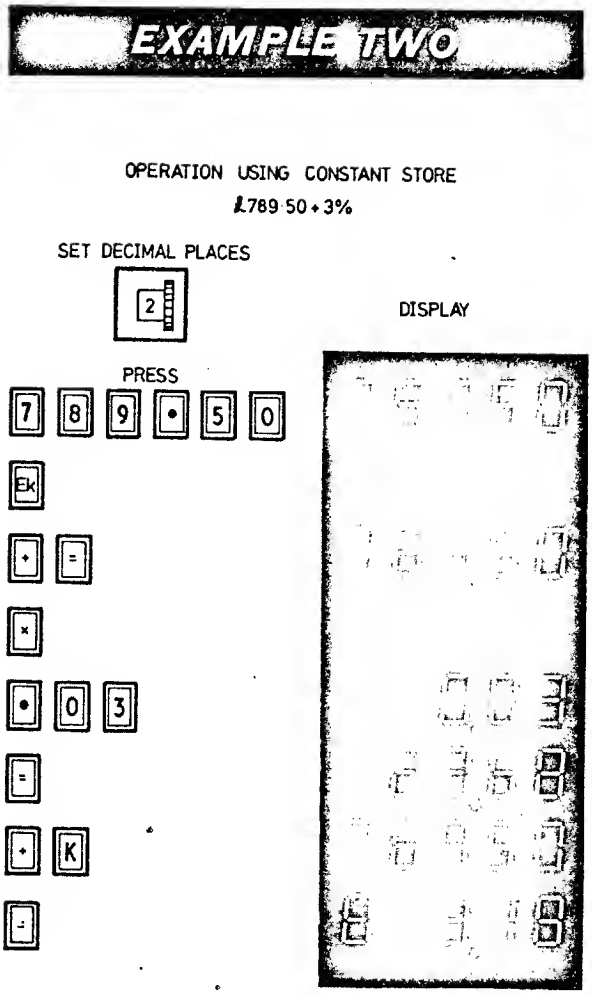


EXAMPLE ONE

This example shows how a simple arithmetical problem can be easily solved using Digi-Cal.

First the number of decimal places required in the answer is set on the decimal place selector. The first number is then entered by pressing the appropriate keys. The add key is then depressed and then the equals key to enter the first number into the calculator. The next number is then entered and added to the previous one by simply pressing the equals key. Similarly with the third number.

We now wish to multiply this total by 0·58 so the multiply key is pressed, 0·58 is entered and the equals key completes the multiplication. The divide key is then pressed, 9·8 is entered and a final press of the equals key completes the calculation.



EXAMPLE TWO

This second example illustrates the use of the stored constant. We wish to add 3% of 789·5 to 789·5. The calculation required is thus 789·5 + (0·03 × 789·5). The number 789·5 is used twice, so to facilitate the calculation it is stored so that it will not have to be entered twice.

Of course, since pounds and pence are involved it is natural to set the number of decimal places to 2. The number 789·5 is then entered but the EK key is pressed before the add and equals keys. The multiply key is then depressed and 0·03 is entered. The equals key then gives 3% of 789·5. Pressing the add and the K key followed by the equals key adds the stored number (789·5) to the previous answer to give the final answer.

PRINCIPLES OF OPERATION

Digi-Cal is built entirely of gates and flip-flops, and operates in a similar manner to the large computers which compile gas bills or calculate wage checks. The main difference is that whereas a large business or scientific computer can be programmed and reprogrammed with ease, Digi-Cal and similar calculators are fixed programme machines, the programme being established at the construction stage.

Another basic difference is that while a large computer performs all its calculations in binary arithmetic, Digi-Cal uses a combination of binary and decimal working known as Binary Coded Decimal arithmetic.

In Binary Coded Decimal (B.C.D.) each decimal digit (e.g. a six or a nine) is represented by a separate group of four binary digits (i.e. 0110 and 1001 respectively). Four binary digits have sixteen possible combinations, but to encode decimal data only the first ten of these are utilised, the other six combinations are redundant and represent invalid data if they should occur.

Representing decimal data using these four bit (bit means binary digit) groups is quite different from their representation using straight binary code as can be seen in the following example:

Decimal	362
Straight binary	101101010
B.C.D.	0011 0110 0010

Binary Coded Decimal operation is used in Digi-Cal because it eliminates a good deal of the conversion circuitry which would be required if straight binary code were to be used for the arithmetic operations, since the input and output data must be in decimal to make it simple for the average user.

B.C.D. ARITHMETIC

Adding in straight binary is very simple and follows the following rules:

$$0 + 0 = 0$$
$$1 + 0 = 1$$
$$0 + 1 = 1$$
$$1 + 1 = 0, \text{ carry } 1$$

With B.C.D. working, a complication arises because although the rules given above do apply when adding individual bits within the group of four digits, as soon as the value of those four digits exceeds nine (not fifteen as in straight binary) a carry has to be generated which is added into the next higher group of four B.C.D. digits. To add 16 and 29 together using B.C.D. we proceed thus:

	DECIMAL		B.C.D.	
1	6		0001	0110
2	9		0010	1001
1	◄		1	◄
4	5, carry 1		0100	0101, carry 1

In Digi-Cal all arithmetic operations can be broken down to the simple processes described above, and the way that this is achieved in practice can be seen by referring to Fig. 1.2 which is the simplified block diagram of the heart of Digi-Cal.

SYSTEM OPERATION

As each key is pressed the numbers are coded into B.C.D. and then enter the Entry (E) register from the right, one after another. When the required entry has been completed the addition is initiated by pressing the "equals" key which starts the programme sequence.

The Z register is first cleared of any data it may contain and then the entire contents of the E register are transferred in parallel to it (6 × 4, 24 bits). It is at this stage of the sequence that Digi-Cal appears in Fig. 1.2.

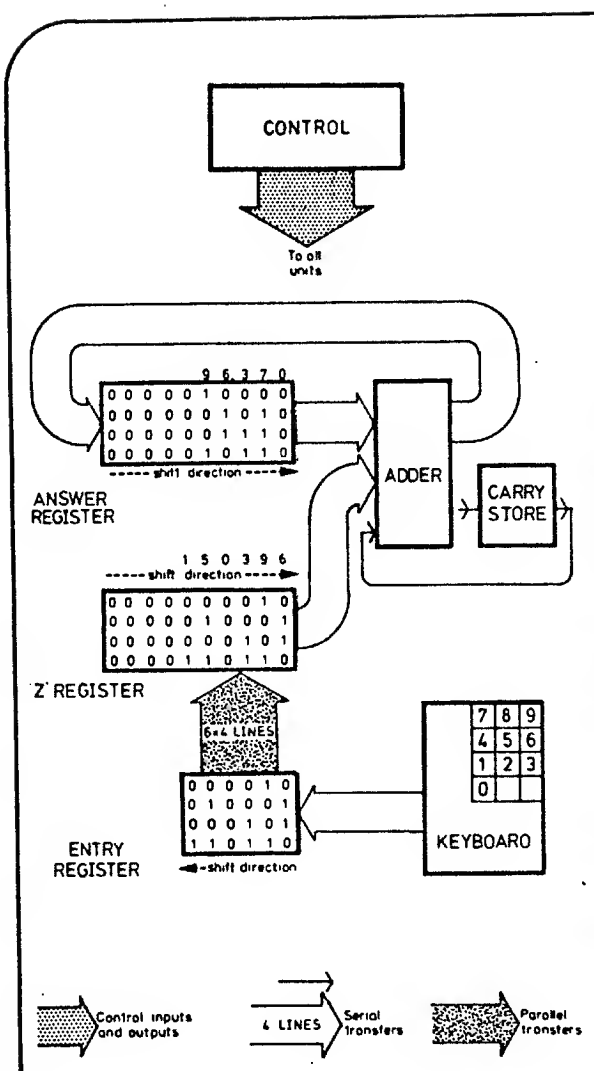


Fig. 1.2. Simplified block diagram of the addition unit

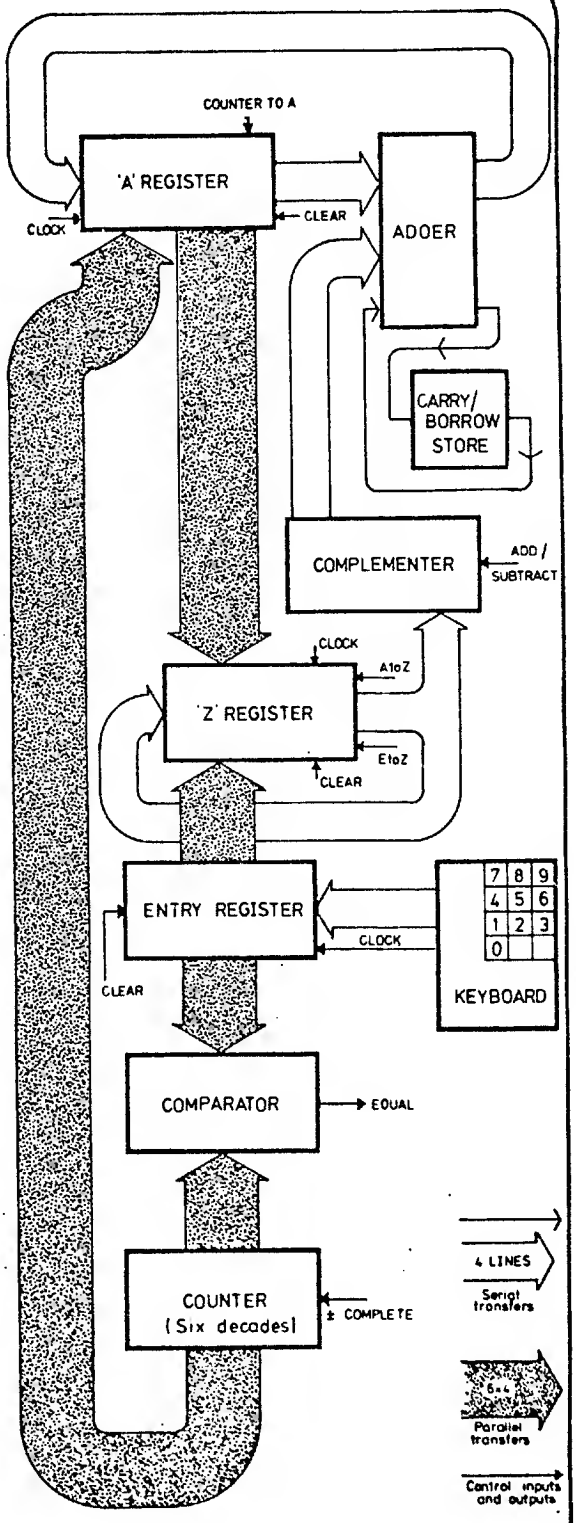


Fig. 1.3. The complete arithmetic unit of Digi-Cal

Both numbers are positioned ready for addition, and to implement this the A register and the Z register are clocked ten times with a burst of ten pulses from the control circuits. Each of the ten pulses presents two new B.C.D. numbers to the adder, which produces a sum and stores a carry if necessary.

When the next pulse arrives the previous answer is shifted into the far end of the A register, so that after the complete addition the first answer is stored in the right-hand location of the A register, and the last answer in the left-hand location, as they should be. In a nutshell then, Digi-Cal carries out parallel B.C.D. but serial decimal addition.

OTHER OPERATIONS

Subtraction is carried out in exactly the same way as addition except that the number to be subtracted is converted to its complement (i.e. each digit subtracted from nine) form before the addition takes place.

Multiplication and division are carried out by performing successive additions and subtractions respectively, and several additions to the basic circuit of Fig. 1.2 are necessary to achieve this. A more complete circuit of the arithmetic section of Digi-Cal is shown in Fig. 1.3. As can be seen, a counter, a comparator and a complementer have been added, along with a number of new interconnections.

MULTIPLICATION

To perform a multiplication the multiplicand is transferred to the Z register from the A register which is then cleared. The multiplier (stored in the E register) is compared with the contents of the counter which is connected to count each complete ten digit addition.

Additions are started by supplying batches of ten clock pulses to the A and Z registers, and this continues until the counter has counted up to the same number as is stored in the E register, whereupon the comparator indicates equality and stops the clock.

The contents of the A register will now be found to be the original contents added to itself the number of times specified by the multiplier, in other words the product of the two numbers.

DIVISION

To perform division, with the dividend in the A register and the divisor in the E register, first the divisor is transferred to the Z register and then the subtractions are started, each one being counted on the counter. When the contents of the A register go negative (determined by the fact that the borrow store is set at the end of a subtraction the clock is stopped and the quotient will be found to be the content of the counter minus 1.

The minus 1 nuisance is neatly disposed of by presetting the counter to 999999 instead of 000000 before counting takes place, the counter therefore automatically counting the number of necessary subtractions minus 1. Finally the quotient stored in the counter is transferred to the A register.

PROGRAMMING AND CONTROL

Up to now the circuits which actually control all the arithmetic and "housekeeping" operations have been ignored, but of course these circuits do have a lot of work to do and are quite extensive.

In Digi-Cal the programme is of the wired diode type, each programme being divided up into a series of time periods (eight steps for add and subtract, and sixteen for multiply and divide). Each programme is enabled when the appropriate arithmetic function is selected, and is started by the equals key.

During any one time step, any of the available programme functions can be performed, depending on whether or not a diode is wired in, and this gives a great deal of flexibility in the finer details of the programme which can be extended or altered at will.

The serial additions or subtractions are carried out at very high speed, the clock frequency being in the region of 1MHz, but the programme steps are performed more slowly, making the programme circuits less critical of wire lengths and board layout. The clock pulses themselves are produced by a board housed in the arithmetic section, this board itself being controlled by the programme.

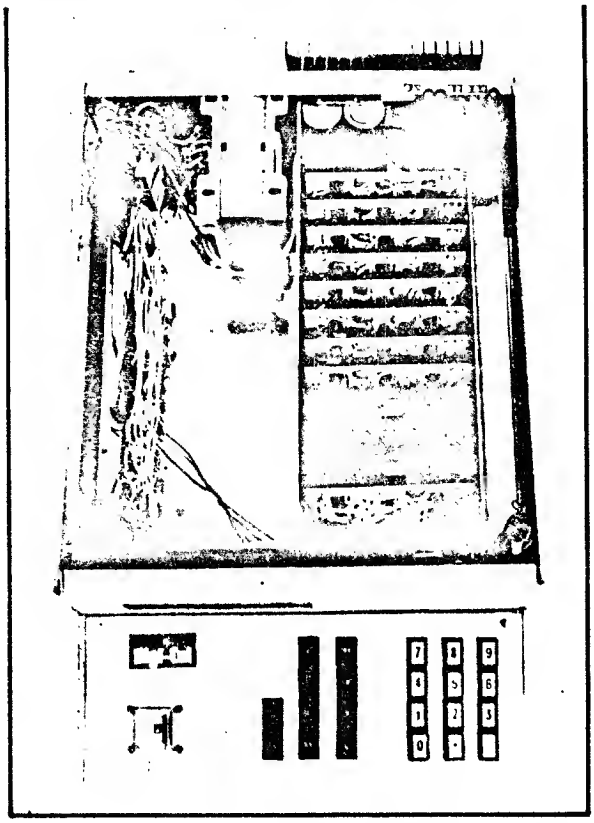
CONSTRUCTION

All the logic used in Digi-Cal is housed on removable boards, the critical arithmetic section on Shirehall DL109 cards, and the display, keyboard and programme on Veroboard panels.

The simple power supplies and regulators are built on a home-etched printed circuit board, the output voltages being five volts for the TTL integrated circuits and 20 volts for the seven segment display.

The keyboard modification to the basic "Contil" case is made with an extra Mod-2 front panel and some ⅛in plywood.

Next month: Construction of main chassis and power supplies, and bulk Component List for the complete project



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PART 2

By R.W.COLES

CONSTRUCTION OF MAIN CHASSIS AND POWER SUPPLIES

AT THE VERY beginning of the design of Digi-Cal it was recognised that a simple and reliable system to house the logic circuitry would be required, and at the same time a pleasing appearance had to be guaranteed so that the completed calculator would not only behave in a professional way, but also look the part.

With the large number of i.c.s involved it was considered essential that as far as possible the individual sections of the calculator should be easily separated by means of plugs and sockets to allow component accessibility, and it was eventually decided that the best way of achieving this was to use a versatile plug-in card system.

Finding a case for the design which would allow the use of plug-in cards and also be easily modified to incorporate a keyboard was quite difficult but eventually the "Contil" Mod-2 type "0" was chosen as the only design type which would fit the bill at a reasonable price.

MAIN CHASSIS CONSTRUCTION

The case for Digi-Cal consists of a "Contil" Mod-2 case with a sloping keyboard attached to the front. The case is supplied in seven sections; four blue panels which form two sides and the top and bottom; two grey panels forming the front and back; and an aluminium chassis plate. An extra grey panel is used to construct the keyboard.

CHASSIS PLATE

The large plate chassis which forms part of the Mod-2 case is a very important structural component of the design because it not only acts as a support for all the logic boards, but also forms a "ground-plane" for the logic interconnections.

The plate is mounted "upside down", that is with the flanges uppermost, in the lowest of the available fixing positions, so as to give sufficient room above it for the plug-in cards.

A large cut-out is made to accommodate the 12 edge connectors used in the design, although, in fact, an extra edge connector position is fully provided for, making 13 in all, to allow for any extra logic circuitry which may be added at a later date (see Fig. 2.1).

Two aluminium sheets are mounted above the chassis to act as supports for the logic cards, the edges of which slide in small plastic guides which are press fitted to the aluminium. In the prototype these aluminium sheets were cut from an extra "Contil" chassis plate, thus removing the need to bend accurate flanges, which are, of course, part of the chassis construction (see Fig. 2.2).

This is a rather uneconomic way of producing these supports although it does yield four quick-release fasteners which were put to good use in the prototype as fasteners for the display and programme Veroboard panels.

At the front of the plate two cuts are made into the aluminium, and the resulting flange is bent down at an angle. This is done to drop the fixing level of the display panel which is mounted in a sloping position to give easy readability from steep viewing angles.

PLUG-IN CARD SYSTEM

The plug-in cards used in the Digi-Cal are Shirehall Dualine type DL109. These are small boards with gold-plated edge connectors of 22 or 44 ways, each having positions for nine dual-in-line integrated circuits.

Integrated circuits with either 14 or 16 pins can be used and each pin position is provided with a printed three hole pad to facilitate wiring up with ordinary connecting wire. In addition to the printed pads, two power rails are incorporated which run past every i.c. position.

Some of the circuits used in Digi-Cal, namely the display, the keyboard, and the programme, did not lend themselves to the Dualine format, and in these cases special designs were made from 0·1in Veroboard which, while requiring extra wiring and hole cutting, provides quite a neat base for the logic.

The edge connectors best suited to the Dualine cards are the type DPK165 which have a full complement of 44 contacts.

The edge connectors are fixed under the chassis plate so that the cards plug in from above. For each socket two ¼in 6B.A. bolts should be used, with two extra nuts and washers acting as spacers to bring the mouths of the sockets flush with the plate and allowing sufficient room for the cards above the chassis.

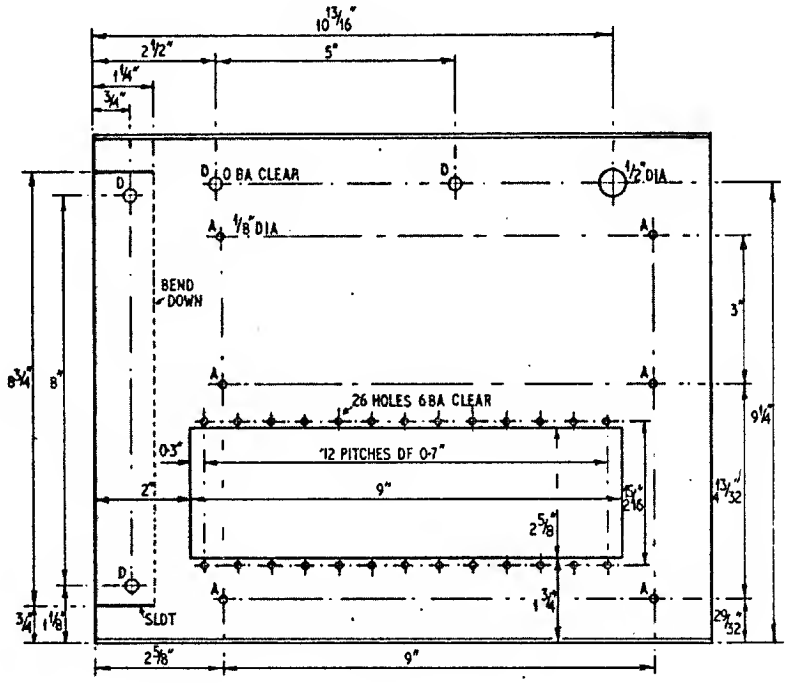


Fig. 2.1. Cutting and drilling details for the main chassis plate. The front is bent down about half an inch to bring the display panel (to be described in Part 3) in line with the front panel

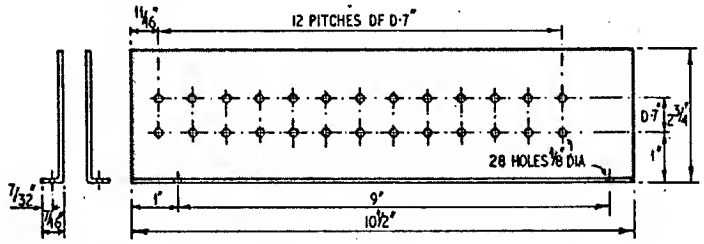


Fig. 2.2. These two plates support the plastic card guides

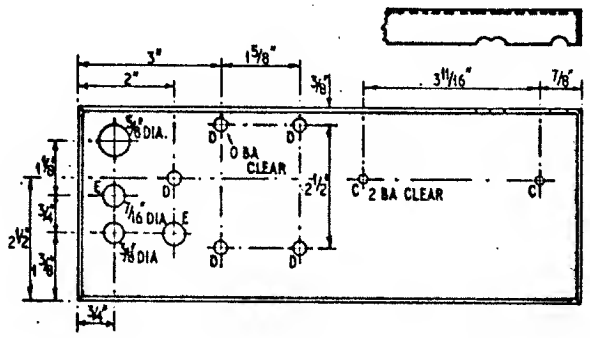


Fig. 2.3. The rear grey panel drilling details viewed from the flange side. Note the semicircular cutouts in the upper flange to allow access to the potentiometers on the power supply board

FRONT AND BACK PANELS

The rear grey panel supports the complete power supply and the drilling is quite straightforward, as shown in Fig. 2.3.

A rectangular hole must be cut in the front panel through which to view the display and the cutting of this should be done carefully. A "nibbling" tool is ideal for this job but if care is taken, sawing and filing will produce satisfactory results (see Fig. 2.4).

OPTICAL FILTERS

The seven-segment incandescent readout devices used on the Digi-Cal display board give the familiar white light output and can be used with a contrast enhancing filter of any colour. The filter material used in the prototype was obtained from West Hyde Developments, the red being found the most appropriate.

Two sheets of filter material are required to give sufficient contrast, one mounted on the inside of the front panel, and the other attached to the front of the display devices themselves.

After the display cut-out has been made in the front panel, the sheet of filter can be glued to the inside with contact adhesive, care being taken not to get any of the adhesive on the visible surfaces, and also to keep the filter as bump free as possible.

If the finishing of the display cut-out has been done carefully there will be no need to use an escutcheon to decorate the outside edges, but a trim can be incorporated if desired.

KEYBOARD CONSTRUCTION

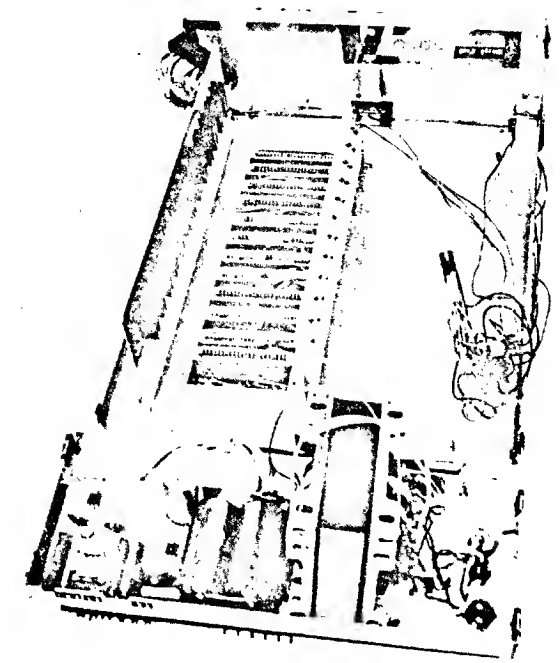
The sloping keyboard attached to the front of Digi-Cal is made from $\frac{1}{8}$in plywood and an extra "Contil" type "0" front panel. The cutting and drilling details for the keyboard are shown in the diagrams (Figs. 2.5 and 2.6) and thanks to the simple fixing method used by the 22 push keys, this potentially tedious task is made easy.

The wooden keyboard frame is fastened to the front panel of the case by means of four wood screws, and provides the necessary solid support for the keyboard proper which is only lightly attached to the frame by two more wood screws to permit its removal when required.

The individual keys are snapped home into the oblong slots in the aluminium, the edges of which may need bevelling to allow them to easily slot into the recesses in the switches.

The lettering and numerals on the key switches is done with Letraset and protected with clear varnish, some experimentation being needed in the number of coats to produce a really durable finish.

The hole for the "decimal point" thumbwheel switch is cut in the same way as the key slots but it is recommended that the holes for the fixing bolts be marked and drilled after the thumbwheel has been inserted as a guide.



A photograph of the power supply unit in the prototype (Note that the bridge rectifier and mains fuse were not included)
The main chassis plate can be seen in this photograph and also the method of mounting the card guide supports

VEROBOARD PANEL

Nearly all the panel interconnections are made under the chassis, and to facilitate this, and to provide spare space for possible additional circuitry, an 11in × 3·7in sheet of 0·1in Veroboard is mounted face up under the chassis alongside the edge connector array.

This panel is spaced from the chassis by two 6B.A. nuts on each of the supporting bolts, the proximity of the chassis being necessary to take full advantage of its ground plane properties.

A sheet of adhesive plastic stuck to the aluminium is advisable to prevent any short circuits when the panel is wired up.

POWER SUPPLY

The construction of the power supply is the first part of Digi-Cal which should be built since the plug-in cards to be constructed need reliable, well regulated power supplies.

The power requirements of Digi-Cal are straightforward: a well regulated five volt supply at 2·5 amps for the logic circuitry; and a 20 volt supply at 200mA for the "Minitron" display devices.

The back panel acts as a support for the entire power supply assembly which is therefore a removable module, only three wires being necessary to connect it to the rest of Digi-Cal.

POWER SUPPLY COMPONENTS

The circuit of the power supplies is shown in Fig. 2.7 and as can be seen, two integrated circuit regulators form the heart of the design.

These devices are both cheaper to buy and simpler to use than their equivalent in discrete components; at about £1·25 each they represent excellent value for money.

The mains input is applied to the fuse and transformer via a "rocker" on/off switch mounted in the extreme corner of the back panel, making operation from the front of the calculator a simple proposition, and retaining the integrity of the power supply "module".

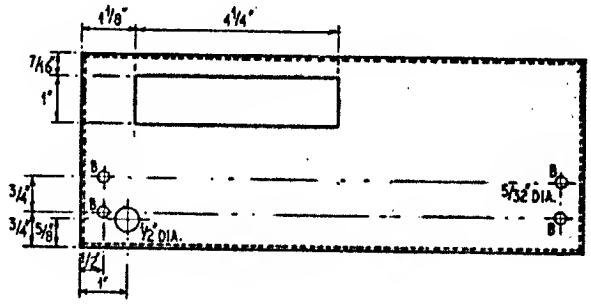


Fig. 2.4. The front grey panel cutting details as seen from the front

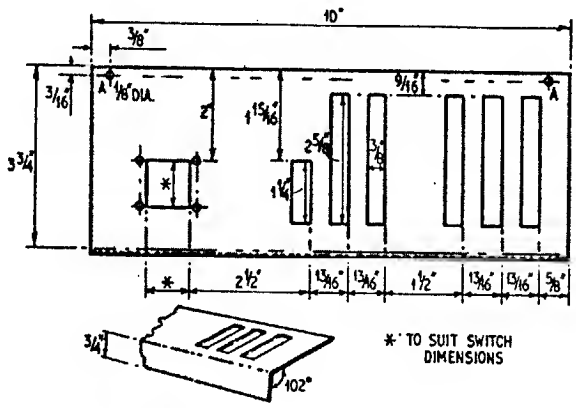
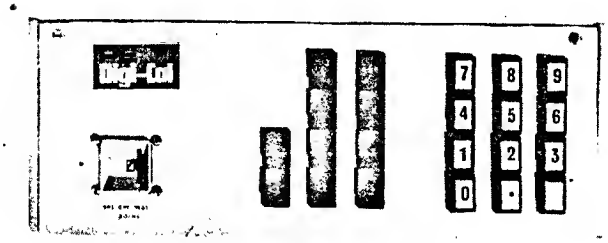


Fig. 2.5. The cutting and drilling details of the keyboard panel which is made from an extra front panel. All flanges should be sawn off except one long edge which is bent as shown in the smaller diagram



The finished keyboard

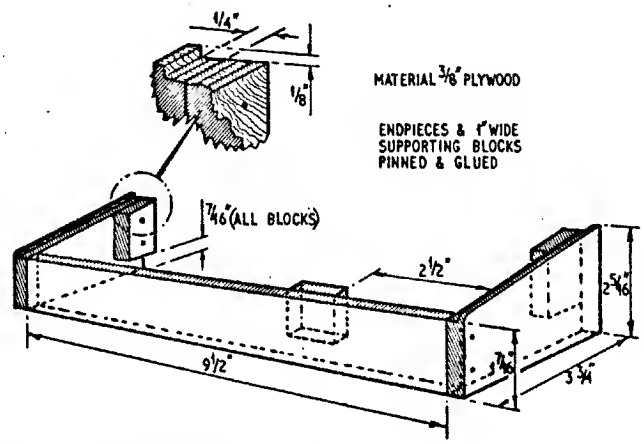


Fig. 2.6. The keyboard supports are constructed from $\frac{3}{16}$in plywood cut as shown

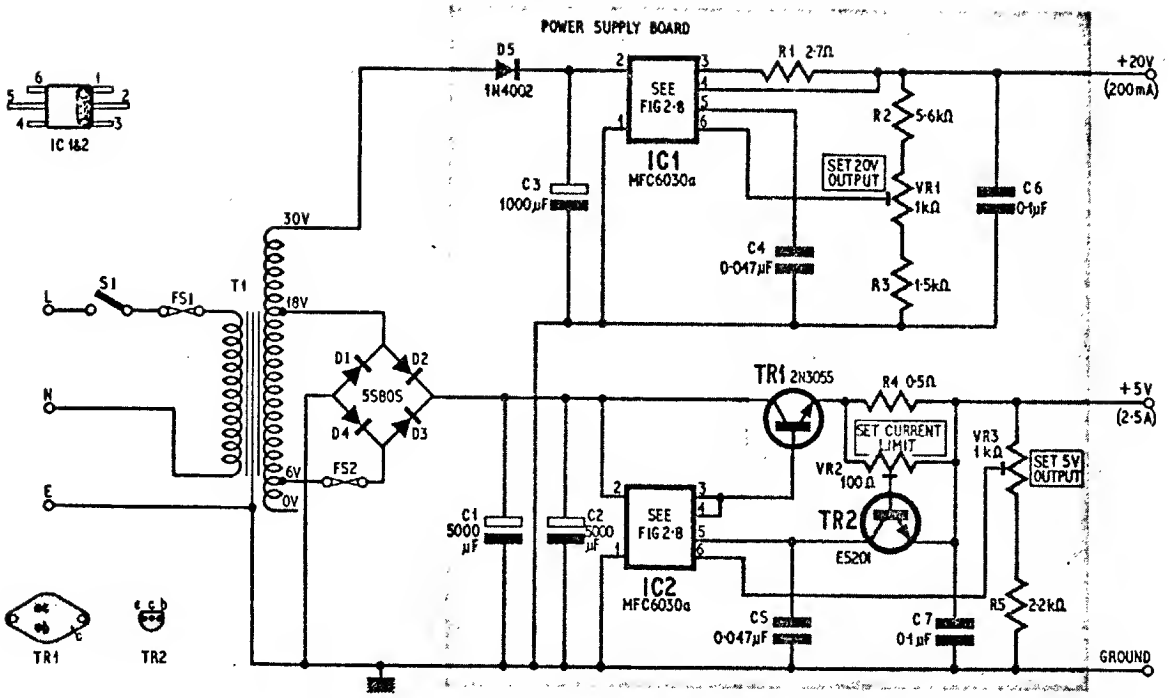


Fig. 2.7. Circuit diagram of the power supply. The internal circuit of the integrated circuits is shown in Fig. 2.8

The transformer itself provides all the necessary voltages and has an internal screen which, when earthed, prevents the capacitive coupling of high-frequency interference into the secondary.

The low voltage supply is rectified by a bridge-rectifier module, which is heat-sinked to the back panel, alongside the transformer.

The circuit diagram of the i.c. regulator is shown in Fig. 2.8. It is a 1 watt regulator, with variable output voltage and current-limiting in a package the size of a pea.

THE 20 VOLT SUPPLY

The 20V supply uses the MFC6030a in its standard configuration, the 24V supply being half wave rectified by diode D5, smoothed by C3 and applied to pin 2 of the i.c. where it is reduced to a stable 20V by the emitter follower action of TRB and TRC.

The base of this compound transistor is driven by the output of the error amplifier TRD and TRE, which compares a fraction of the output voltage provided by the potentiometer chain, R2, VR1 and R3 with a stable reference voltage generated by a Zener and diode/transistor combination, DA, TRA, DB, C and D. Any difference detected by the error amplifier causes either more or less base current to be supplied to the compound transistor to bring the output voltage back to its preset level.

Current-limiting is provided by TRF working in conjunction with an external programming resistor, R1, which is chosen so that when the desired maximum current is reached, the voltage across the resistor is sufficient to turn on TRF and divert the drive current which would otherwise feed the base of TRB.

Capacitors C4 and C6 help to stabilise the regulator so that no high frequency oscillation can occur under transient conditions.

THE FIVE VOLT SUPPLY

The basic i.c. regulator can only supply a maximum of 200mA to an external load, so with the five volt supply the output of the i.c. is used to drive the base of a 2N3055 power transistor, thus expanding the current handling capacity of the circuit up to the required 2·5 amps. The 2N3055 has to dissipate about 15 watts under operational conditions and is therefore mounted outside the case on a substantial heatsink.

The internal current limiting circuit cannot easily be used with an external power transistor, but by using a single *npn* transistor (TR2) current limiting can be retained.

In this supply variable current limiting is achieved by tapping off a variable fraction of the

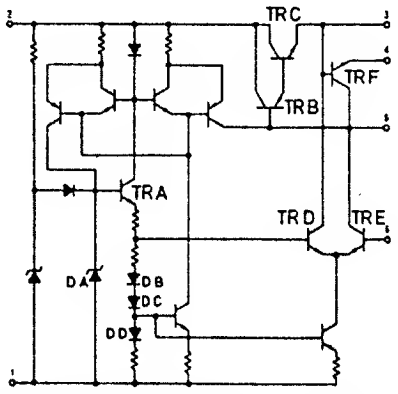
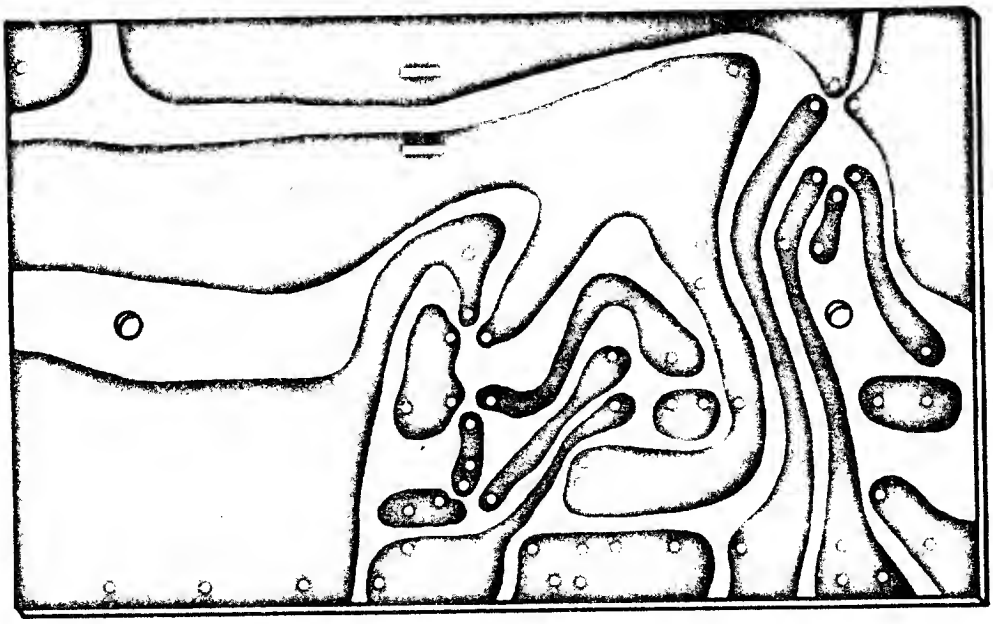


Fig. 2.8. The internal circuit diagram of the Motorola MFC6030a regulator i.c.



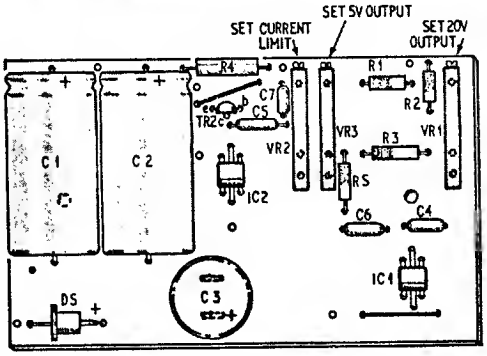
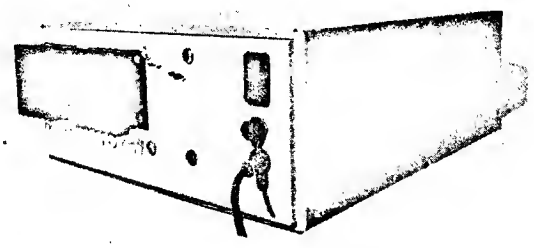


Fig. 2.9. Component layout and wiring of the board. The printed circuit pattern is shown full size above



A rear view of Digi-Cal showing the power supply transistor on its heatsink

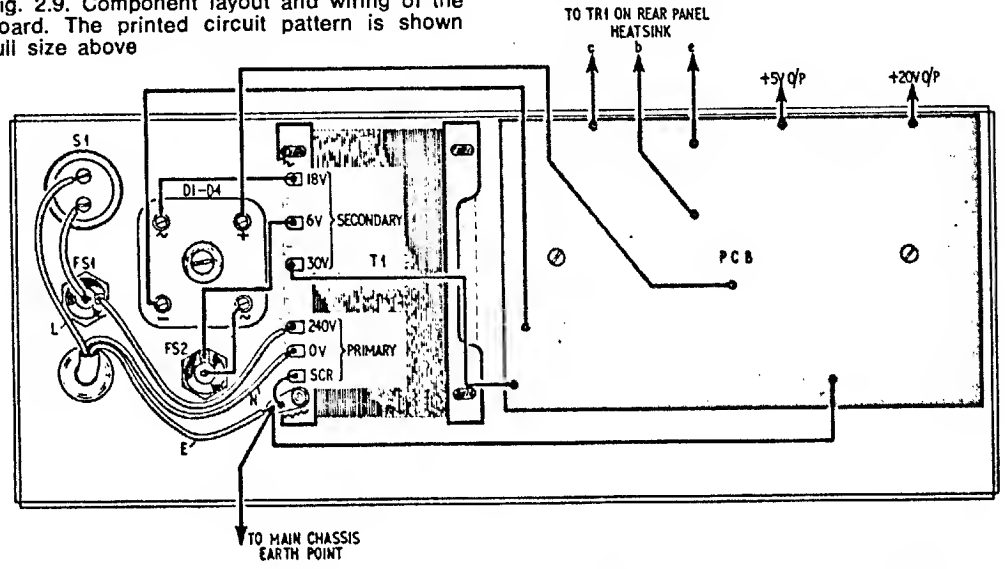


Fig. 2.10. Interwiring diagram of the complete power supply unit

voltage dropped by the current limiting sense resistor R4, by means of the potentiometer VR2.

The other components used in the 5V circuit perform similar functions to their counterparts in the 20V regulator.

PRINTED CIRCUIT MAKING

The power supply components, with the exception of the 5V series regulator transistor and transformer, are all mounted on a home-made printed circuit of simple design.

The use of a printed circuit is made necessary partly by the awkward shape of power supply components in general, and also by the high currents which are carried by some of the printed tracks.

The etching of the circuit is simply achieved by painting on the conductor pattern shown in Fig. 2.9 with quick drying paint, and then immersing the copper laminate in solution of 60 per cent ferric chloride, obtainable from good chemists.

COMPONENTS

CASE AND KEYBOARD

Contil Mod-2 type "0" case with extra front panel and either an extra type "0" chassis or a sheet of 18 s.w.g. aluminium (see text), ¼in plywood for the keyboard support

POWER SUPPLY MODULE

Resistors

R1	2·7Ω	R4	0·5Ω 3W
R2	5·6kΩ	R5	2·2kΩ
R3	1·5kΩ		

All ±10%, ¼W carbon unless otherwise stated

Potentiometers

VR1 1kΩ lin. preset
VR2 100Ω lin. preset } All Bourn's "Trimpot"
VR3 1kΩ lin. preset

Capacitors

C1, C2 5,000μF 15V elect. (see text) (2 off)
C3 1,000μF 25V elect.
C4, C5 0·047μF (2 off)
C6, C7 0·1μF (2 off)

Transformer

T1 Mains transformer, secondary 0–6–10–15–18–30 2A (West Hyde Developments type TRB)

Transistors

TR1 2N3055 TR2 E5201 (West Hyde)

Diodes

D1–4 5SB05 bridge rectifier (I.R.)
D5 1N4002 or any 100 p.i.v. 1A diode

Integrated Circuits

IC1, IC2 MFC6030a (2 off)

Switch

S1 On/off switch (Bulgin type S1B825)

Miscellaneous

FS1 2A fuse and holder (Belling Lee L575)
FS2 2·5A fuse and holder (Belling Lee L575)
Heatsink for TR1 (Marex type 10DN0200A300 or similar)
5in × 3in copper clad laminate

When all the unpainted copper has been dissolved by the etchant (about half an hour) the circuit can be washed and the paint removed with scouring powder to reveal the bright copper conductors.

Hole drilling is best completed with a drill about 1mm in diameter, after the hole pattern has been checked for accuracy with the actual components to be used, as some size variation of things like electrolytics and potentiometers is inevitable.

Smoothing of the low voltage supply is achieved by two 5,000μF capacitors in parallel, the large total capacity being necessary because of the high currents involved. The precise total value is not critical, and anything larger than 6,500μF will suffice; the most critical feature of these capacitors is their size, very little room being available on the printed circuit.

MOUNTING THE BOARD

The power supply printed board is mounted above the chassis line in the back panel by means of two 2B.A. bolts, spacing from the panel being achieved with two or three extra nuts. With this amount of spacing the potentiometers are not accessible from above, and it is necessary to file three semicircular cutouts in the back panel as shown in Fig. 2.3.

The heatsink used in the prototype was one of the type commonly used in audio amplifiers to mount two output transistors, this was cut in half and mounted on the outside of the back panel by means of four 6B.A. bolts. The actual heatsink used is not important provided that it has at least 30 square inches of surface area exposed. The 2N3055 must be insulated from the heatsink using the usual mica washer and bushes provided with the device when purchased.

Interwiring is carried out as shown in Fig. 2.10.

TESTING THE POWER SUPPLY

When the power supply module has been assembled it can be tested by plugging it into the mains supply and connecting a voltmeter to the output of each supply in turn. The potentiometers should all be set to mid-travel before the mains is switched on, and the voltages measured should be fairly close to their required value, accurate setting being made with the appropriate potentiometer.

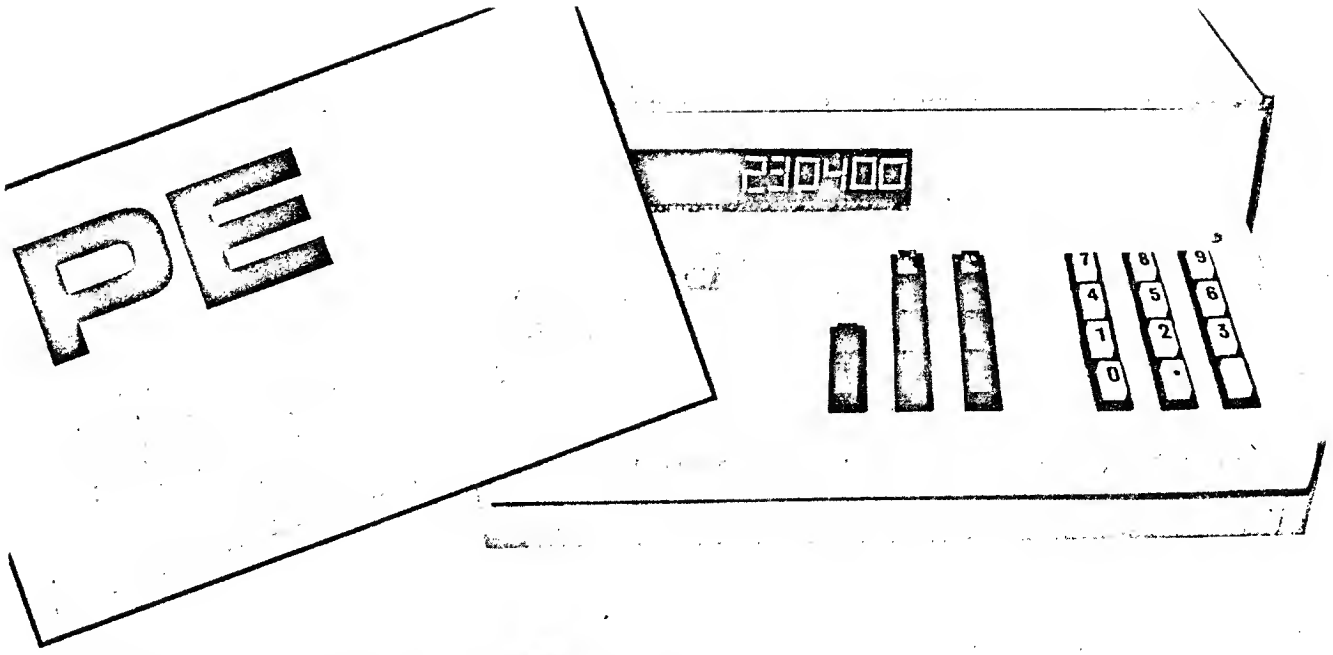
The current-limiting for the 20V supply is preset and should not be tested by shorting out the supply, as it will only safely handle brief short circuits of the type which can occur accidentally whilst wiring up.

The current limiting of the 5V supply is able to handle continuous short circuits, and the threshold value can be set by connecting an ammeter across the output terminals of the supply and adjusting the current limit potentiometer until a reading of 2·5 amps is obtained.

The 2·5 amp setting is required for the finished calculator, but if the supply is going to be used to check each separate board as it is completed the current limit can be set to suit each situation, thus avoiding any spectacular shorts!

It should be noted that several of the power supply components, including the 20V regulator i.c., do get quite hot in operation: this is quite normal and constructors can rest assured that all components are operated well within their maximum ratings.

Next month: Construction of display panel



BULK COMPONENT LIST . . .

Below is the complete list of components used in Digi-Cal (excluding the power supply).

Individual component lists will, of course, be published with circuit diagrams as they appear.

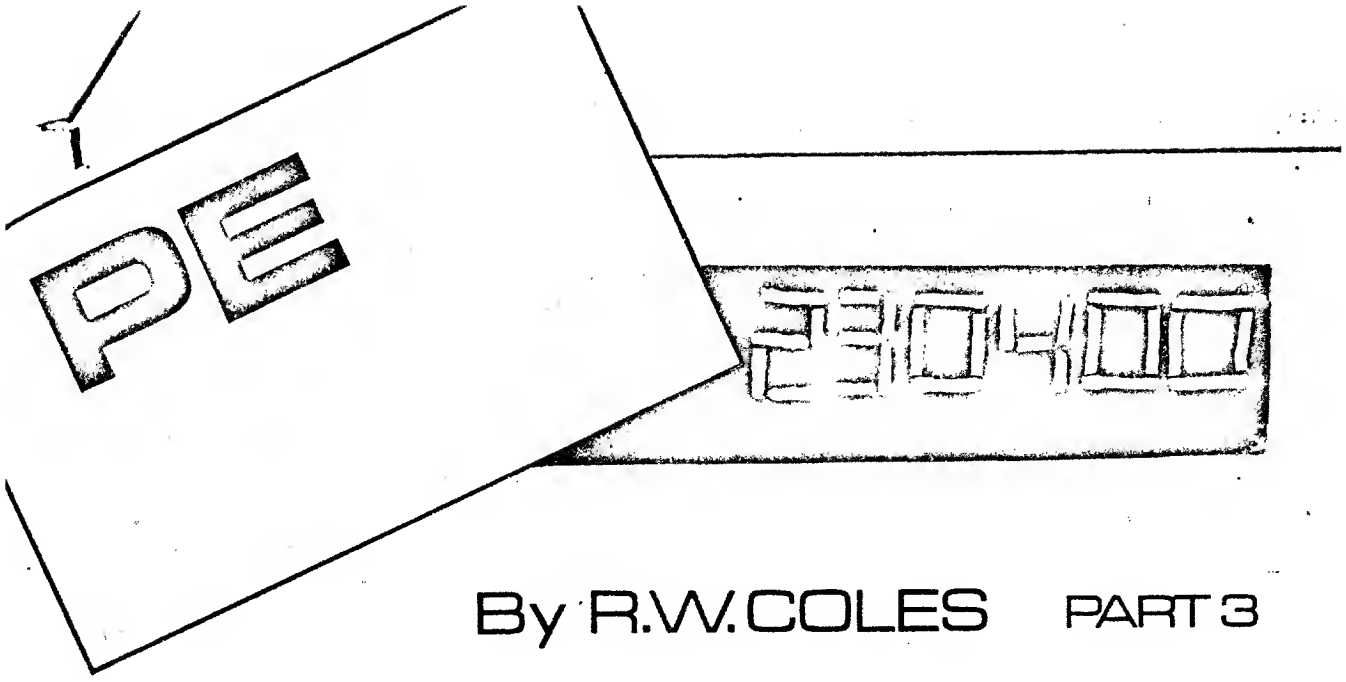
The estimated total price for all components is £110, assuming bulk purchase.

Prices can be kept to a minimum by buying in large quantities and the following firms have kindly agreed to supply all digital integrated circuits and display devices at a reduced price, if bought as one package: Bi-Pak Semiconductors, Chromasonic Electronics, Electrovalue, Henry's Radio, L.S.T. Electronic Components, A. Marshall & Son, G. W. Smith & Co. (Radio), and Trampus Electronix. (For addresses see advertisements)

Integrated Circuits	Quantity
SN7400	11
SN7401	23
SN7402	1
SN7404	2
SN7405	6
SN7408	1
SN7410	7
SN7413	1
SN7420	1
SN7440	8
SN7442	3
SN7445	1
SN7446	1
SN7450	4
SN7474	21
SN7475	6
SN7483	3
SN7486	8
SN7490	12
SN7493	1
SN7494	8
SN7496	8
SN74119	1
SN74121	2
SN74151	1
SN74154	2
SN74191	1

Resistors	Quantity
47Ω	15
560Ω	3
1·2kΩ	25
3·9kΩ	1
5·6kΩ	26
15kΩ	1
180kΩ	1
Capacitors	
0·001μF	4
0·01μF	1
0·047μF	21
0·1μF	7
10μF 15V elect.	17
22μF 15V elect.	2
150μF 15V elect.	1
Transistors	
E5200	9
E5201	10
Diodes	
General purpose silicon (West Hyde type "red")	145

Plug-in Logic Cards	
Shirehall Dualine:	
DL109/22	5
DL109/44	7
DL107/44 (optional)	1
Edge Connectors	
Shirehall DPK165	12
DL131 card guides	3 packets
Seven Segment Indicators	
Minitron 3015F	8
Key Switches	
Bulgin type MP22 white	12
black	9
Lampholder	
Bulgin type D22	
Thumbwheel Switch	
Birch-Stolec type EB10N 1248 – a pair of end plates	1



By R.W. COLES PART 3

CONSTRUCTION OF THE DISPLAY PANEL

LAST month the construction of the main chassis was described. In this month's part the logic and construction of the display panel will be dealt with. The outputs from the power supply whose description also appeared last month will be used when it comes to the testing stage.

DISPLAY BOARD

Any calculator depends heavily on its display system not only because it is obviously necessary to register the answers to the problems being worked out, but also because it is required to display any data entered through the keyboard so that keying errors can be corrected immediately.

Digi-Cal has an entry capacity of six digits and an answer capacity of up to eight digits, making a display length of eight digits necessary. In addition to the display of numerical data the display is required to illuminate a decimal point in any one of four locations, the exact position being determined by the setting of the decimal point thumbwheel (for answers) and the contents of the decimal place counter (for entries).

The display format chosen for Digi-Cal is the "seven segment" system specified because of its simplicity and low cost.

With any display format, but particularly with the seven segment system, a multi-digit readout can look confusing if insignificant zeros are not blanked in some way to leave the significant digits uncluttered. For Digi-Cal a leading-edge ripple blanking circuit has been incorporated which produces a very easily interpreted display of the form normally used in written calculations.

DISPLAY DEVICES

When choosing the display devices three different types were considered, the gas-filled Nixie tube, the Light Emitting Diode (L.E.D.) and the incandescent filament.

Nixie tubes were rejected because of their bulkiness and high-voltage requirements and L.E.D.s because of their high cost. The device eventually selected was the Minitron type 3015F which is an incandescent filament, seven-segment readout with a built in decimal point, housed in a package with the same pin configuration as a dual-in-line integrated circuit.

GLOSSARY OF TERMS USED

CALL-UP bring data from a store or register
ENABLE allow the inputs or outputs of a device to become active. Also the reverse **DISABLE**
DATA BUS a wire or group of wires used to carry data to or from a number of different locations (see TIME SHARING)
DUMMY INPUT a temporary input to a device used to simulate an input that could occur (Note that with TTL I.c.s. an input with no connections to it will be equivalent to a logic 1)
RIPPLE BLANKING or ZERO SUPPRESSION the method of improving readability by switching off, i.e. blanking, all display devices whose inputs are insignificant zeros.
DIODE MATRIX a two-dimensional array of diodes used for a variety of purposes such as decoding and read only memory
READ ONLY MEMORY a system whereby unalterable data is held in store to be called up when required
ONE-OF-EIGHT or ONE-OF-TEN DECODER a decoder which takes a binary number as its input and produces only one active output (out of eight or ten) as its output
DECADE COUNTER a system which has ten states each of which is produced in turn when clock pulses are present at its Input
CLOCK a system which produces pulses of fixed duration at a fixed repetition rate
TIME SHARING or MULTIPLEXING the method of selecting data from a number of sources in turn and presenting them on a single wire or group of wires
STROBE PULSE a pulse which enables a system for a fixed period only

The small size and low current requirements, along with their ready availability made the Minitron indicators ideal for the display, and ensured that both the indicators and the drive electronics could be built on the same piece of Veroboard, eliminating all of the messy readout-to-board wiring required with most systems.

DRIVE ELECTRONICS

The Minitron indicators are used in Digi-Cal as part of a completely self-contained display board working in the "time shared" mode.

Time sharing, or multiplexing the indicators in a display system involves scanning each digit of the display in turn, and switching it on for only a fraction of the total display period.

The basic principles of time shared displays were laid out in last month's article in the *Alpha Numeric Displays* series, and for this reason we need only discuss them briefly here.

One of the advantages of a multiplex system is that only one seven-segment decoder is required, instead of one per digit as in a static system. The single decoder is connected to each digit of the display in turn by means of an electronic commutator which at the same time calls-up the data to be displayed in that digit position from its stored location.

The scanning rate is made high enough that no flicker is detected by the human eye, and the energising voltage of the indicators is increased from its nominal d.c. value to compensate for the fact that each indicator is on for only a short time compared with the time it is off.

Another advantage of time sharing is that since all the data for display is not required simultaneously, connections between the data store and the display can be made by means of a time shared "data bus" (see *Alpha Numeric Displays*, Pt. 6) consisting of only four wires in this case.

BLOCK DIAGRAM DETAILS

The skeleton block diagram of the display system is shown in Fig. 3.1.

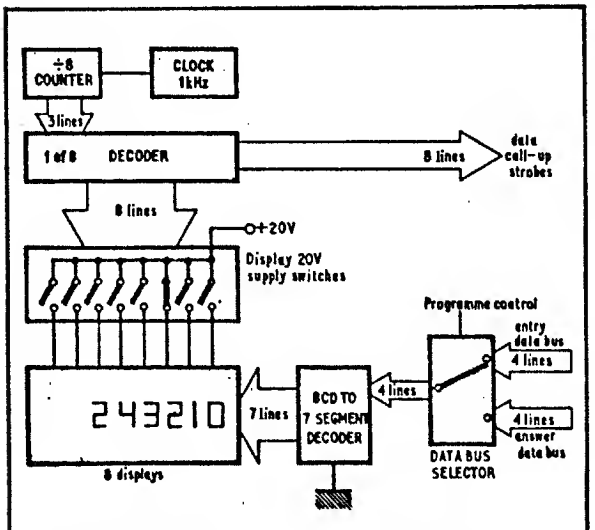


Fig. 3.1. Block diagram showing the main sections of the display panel

The 1kHz clock is used to drive a binary counter whose own outputs are fed to a decoder which produces a one-of-eight response to drive the electronic switches which connect the 20 volt line to the Minitron common terminals.

The one-of-eight output is also used to "call-up" each bit of the data in turn from the entry and the answer registers of the calculating unit. Both the entry and the answer data buses are routed to the display board where one of the two is selected for display by a gating arrangement controlled by the programme.

The selected data is fed to a seven segment decoder which produces as its output a series of "earth" connections corresponding to the segment pattern for that numeral.

The seven outputs from the decoder are wired to all the Minitron segment wires (via an isolating diode matrix) but since only one of the Minitrons will be connected to the 20 volt supply only that device will indicate the data on the bus. In the following time period of course, a different Minitron will be "enabled" and a different B.C.D. code will appear on the bus.

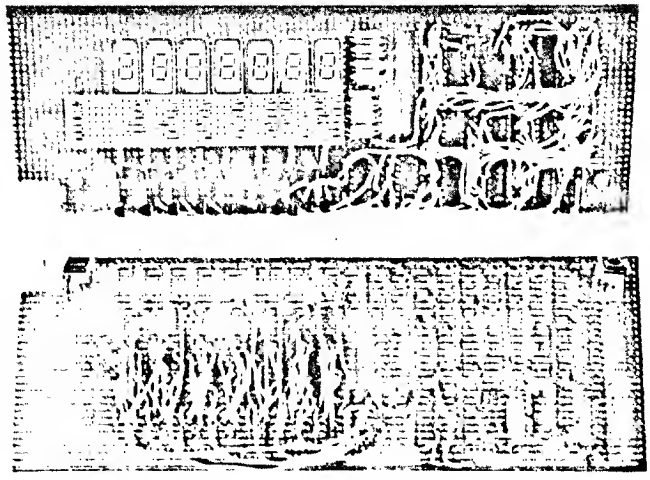
CIRCUIT OPERATION

The circuit of the display is shown in Fig. 3.2, and before going into a detailed guided-tour it would be useful to spend a while correlating the various components on the circuit with their counterparts in the block-diagram (but note that a few of the components cannot be found a home in this way).

In the detailed circuit the clock (Fig. 3.3) is used to drive an SN7490 (IC6) decade counter which has its D output connected to the RESET input so that as soon as a count of eight appears the counter is reset to all zeros from which it starts to count up again.

The output from the SN7490 is decoded by an SN7442 one-of-ten decoder (IC5), which in this case is made into a one-of-eight version by connecting its D input to earth permanently.

The SN7442 outputs are "active low" which means that all outputs except the energised one will be in



Photographs of the two sides of the Veroboard panel in the prototype. Construction is complete except for one Minitron. Note the underside wiring from the diode matrix to the Minitrons

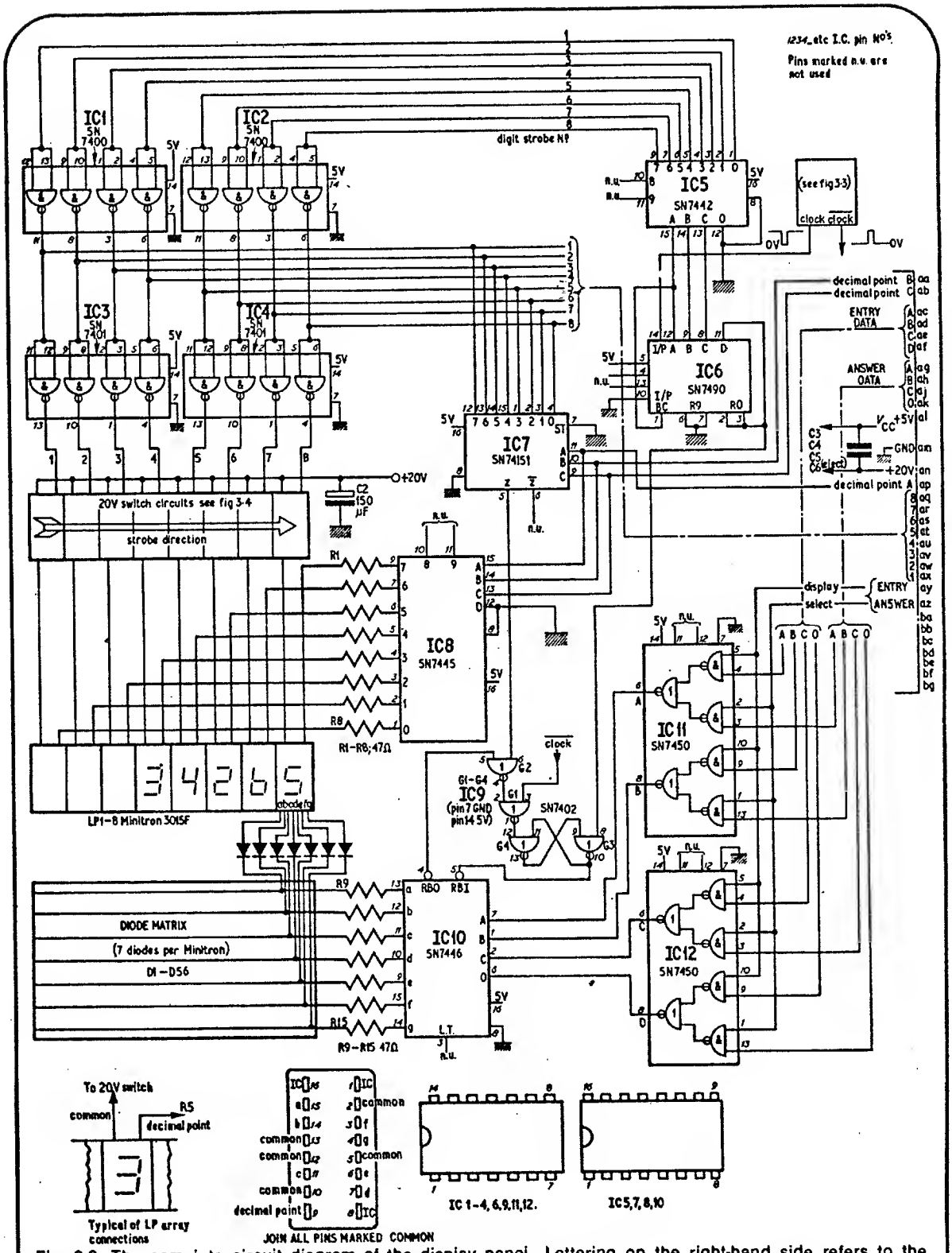


Fig. 3.2. The complete circuit diagram of the display panel. Lettering on the right-hand side refers to the copper strips as shown in Fig. 3.5

the "logic 1" state. This is the wrong sense to drive the following circuits so two quad NAND gates IC1, IC2 (SN7400) are used as inverters to give a one-of-eight eode which is "active high".

The eight lines so produced are used both to drive the eight electronie switches routing the 20V supply to the selected Minitron, and to eall-up the eorreet data from the remote storage registers.

ELECTRONIC SWITCH

The eircuit of each of the eight 20 volt switches is shown in Fig. 3.4 along with one of the eight open-collector gates used to drive it.

The SN7401 gates also act as inverters so that the selected gate will have an "active low" output, or in other words, a low impedance earth connection, this earth eonnection being used to turn on the *pnp* switch via a resistor and Zener diode.

The Zener diode is used to proteet the output transistor of the gate which has quite a low collector breakdown voltage of about 15 volts. The Zener aetually employed in this position is the reverse biased base emitter junction of an *npn* transistor with a breakdown voltage of about 6·5 volts: using a transistor instead of a purpose-built Zener is aetually cheaper where voltage toleranees are loose.

It is worth noting that the breakdown voltage of SN7401 gates is not guaranteed above seven volts by the manufaeturers, but in tests these gates have nearly all shown breakdowns of 15 volts or more which is satisfactory for these purposes, and should a particularly poor device be found (this will be indieated by its digit being "on" permanently) the gate can be replaced.

DATA BUSES

Returning to the main circuit, the two data buses are fed to four AND-OR-INVERT gates IC11, IC12 (2 × SN7450) whieh aet as four single pole ehange-over switches with the extra feature that they also invert the data on the buses, a desirable feature in faet, since this data is in eomplement form to start with.

Seleetion of the required data bus is performed by two eontrol wires which come from a bistable in the control programme, the selected bus being fed from the SN7450s to the SN7446 seven segment decoder inputs (IC10).

Each of the SN7446 outputs corresponds to one of the display segments labelled "a" to "g", and these outputs are wired to all eight of the appropriate segment connections on the Minitrons via a diode matrix and current-limiting resistors.

The diode matrix is neeessary to ensure isolation between the separate indicators, and consists of one diode for each segment of each Minitron, making 56 in all.

The eurrent-limiting resistors are included to limit the high inrush of current to the outputs of the decoder possible when an indicator is first switched on and is cold. Since the output of the deeoder is subjeet to eontinuous switehing in a time shared system these resistors are vital.

DECIMAL POINT

The deeimal point in the Minitron indieator is effectively an extra segment, one of its eonneetions being made to the COMMON terminals, and the other being available for eontrol purposes.

In the Digi-Cal system the control wire for the selected decimal point is grounded through a one-of-eight decoder, the filament being switehed on along with the appropriate numeral segments when the correet digit-strobe is present and the COMMON terminal simultaneously connected to the 20V supply.

The required position of the decimal point is defined by a three bit binary code which can originate in one of two places the appropriate one being selected in the keyboard circuit by the eontrol programme.

The three wires bringing the code to the display earry it in inverted form so that 111 means "no deeimal plaees" and 000 means "seven deeimal places".

The three bit binary number is fully deeoded to its one of eight equivalent by an SN7445 decoder (IC8) and the appropriate eonnections made via eurrent-limiting resistors to the deeimal point control lines on the Minitrons.

Eight separate decimal point positions are not required by the arithmetie section of Digi-Cal which as it stands can only eope with four separate deeimal points.

The display unit is wired for eight positions, firstly to allow for improved calculating circuitry and secondly to make the display a self-contained system whieh ean be used for any other purpose should this be required.

If desired by the constructor, the few extra wires redundant in Digi-Cal can be left out as well as R1 to R4.

RIPPLE BLANKING

Up to now the ripple blanking eircuitry (IC9 and IC7) has been ignored, and this has been done beeause it is essentially an "add on extra" feature making it possible to leave it out altogether without affecting the operation of the rest of the circuit.

Despite the fact that it is optional, however, it must be said that the display readability is sadly redueed without it and its incorporation is highly reeommended.

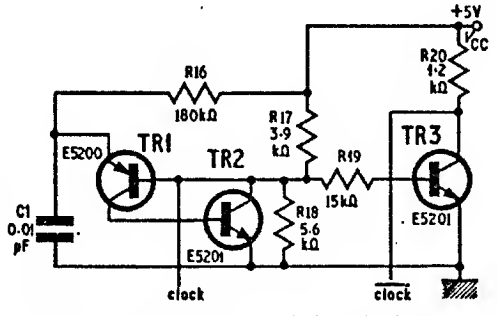


Fig. 3.3. Circuit diagram of the clock generator circuit

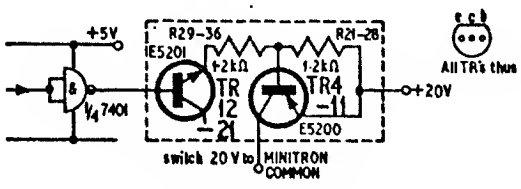


Fig. 3.4. Circuit diagram of the 20V switching circuits, eight of which are required

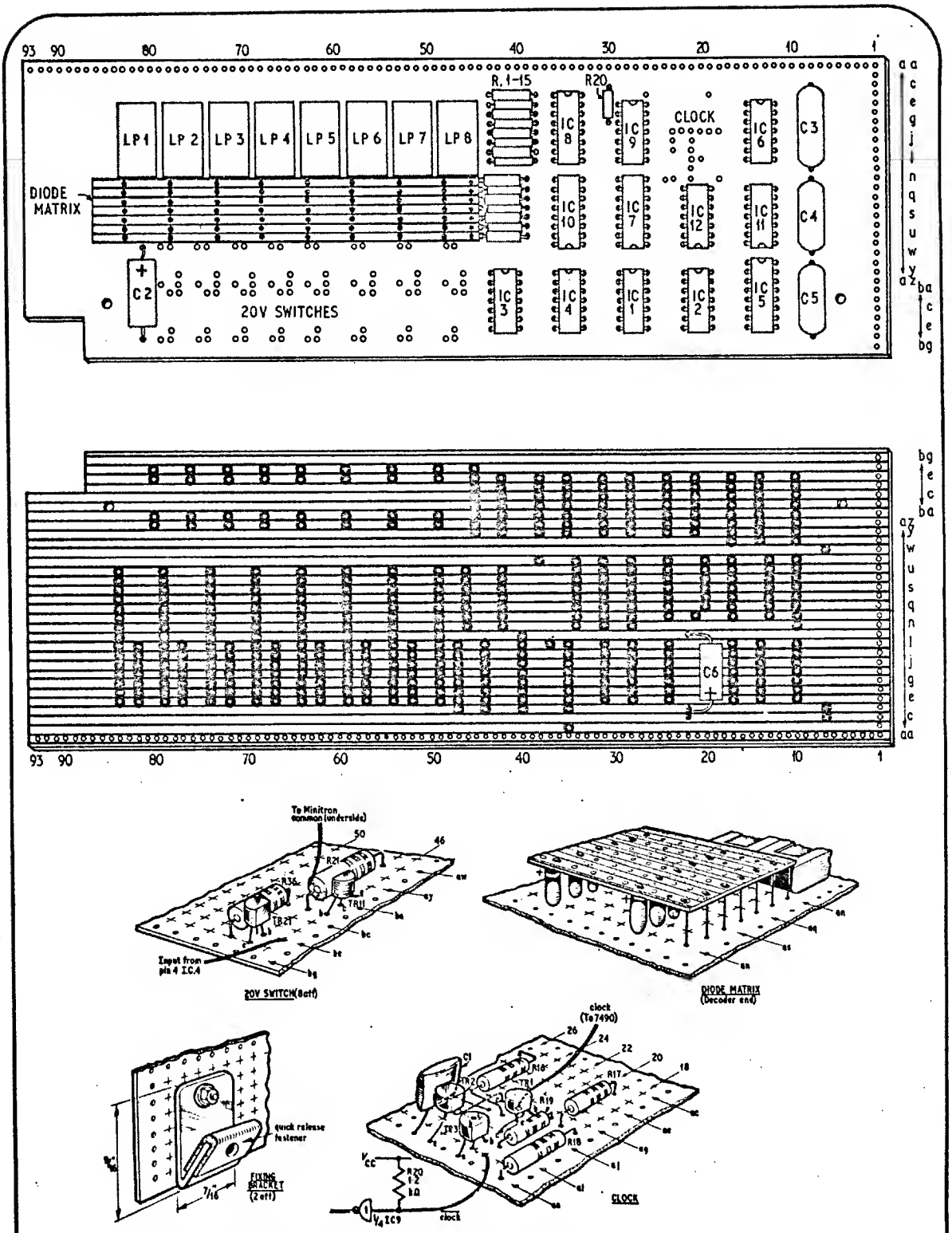


Fig. 3.5. Component layout and copper strip breaks for the Veroboard display panel. Details of the construction of the clock, diode matrix and 20V switches are shown in the smaller diagrams

In a time shared system the ripple blanking information has to be stored for future use with subsequent digits as they arrive on the data-bus, and in the Digi-Cal display this storage is effected by means of a "custom-designed" flip-flop in the form of an SN7402 quad two input NOR gate, IC9.

The display strobing system operates from left to right across the display, the most significant digit being displayed first, and as each digit is decoded by the SN7446 an extra output is produced for use in the ripple blanking circuit.

This output is a "zero detect" output which will go low if the data at the input of the decoder is 0000. If this ripple blanking output is low at the start of a strobing run across the display then that first digit is blanked by a low input to the decoder's ripple blanking input and at the same time the fact that this digit is a zero is "remembered" by the SN7402 flip-flop.

If the next digit is also a zero it will be blanked in turn and so on until the first significant number appears at the decoder inputs at which time the flip-flop will be set by the corresponding high output on the ripple blanking output (RB0) pin.

From this point on, any digit, regardless of whether it is a zero will be displayed until the flip-flop is reset by the strobe counter reset pulse at the end of a run.

DECIMAL POINT ZEROS

The system as just described performs the suppression of all leading edge zeros as required, but can give peculiar results in some conditions.

If the answer or entry to be displayed consists of all zeros for example then they will all be blanked to give a display consisting of nothing but a decimal point, an obviously unsatisfactory state of affairs, and one which can be corrected by arranging to have the ripple blanking flip-flop set by either the appearance of a significant digit *or* the appearance of the digit immediately preceding the decimal point even though it be a zero, whichever arrives first in each display run.

With this proviso an eight digit answer consisting of all zeros would be displayed as 0·00 (two decimal places selected).

Arranging for the ripple blanking flip-flop to be set in this way is quite straightforward except for the fact that the decimal point position can be in any one of eight places, a complication which is overcome by the use of an SN74151 eight line to one line multiplexer (IC7).

This device operates in a similar manner to a one pole eight way switch, the switch position being determined by the three bit binary code input, which in this case is the decimal point position code.

The eight inputs are provided by the display strobes, only one of which will be selected by any particular code for transmission to the Z output. When the selected strobe appears it is routed straight to the flip-flop SET input and it removes the blanking signal until the end of the display run when the flip-flop is reset and the process repeated.

CONSTRUCTION

The baseboard for the display consists of a single piece of Veroboard cut from a West Hyde type 122 board which has a matrix of 0·1in.

COMPONENTS

DISPLAY PANEL

Resistors

R1–15	47Ω (15 off)
R16	180kΩ
R17	3·9kΩ
R18	5·6kΩ
R19	15kΩ
R20–36	1·2kΩ (17 off)

All ¼W, ±10% carbon

Capacitors

C1	0·01μF
C2	150μF 15V elect.
C3–5	0·047μF (3 off)
C6	10μF 15V elect.

Transistors

TR1	E5200
TR2, TR3	E5201 (2 off)
TR4–11	E5200 (8 off)
TR12–21	E5201 (8 off)

All West Hyde types

Diodes

D1–D56 West Hyde type "red" (56 off)

Integrated Circuits

IC1, IC2	SN7400 (2 off)
IC3, IC4	SN7401 (2 off)
IC5	SN7442
IC6	SN7490
IC7	SN74151
IC8	SN7445 (*or* SN74145 see text)
IC9	SN7402
IC10	SN7446 (*or* SN7447 see text)
IC11, IC12	SN7450 (2 off)

Display Devices

LP1–8 Minitron 3015F (8 off)

Miscellaneous

0·1in matrix Veroboard (9·3in × 3·3in)

The dimensions of this board along with the copper strip break layout are given in Fig. 3.5.

The component layout is also shown in Fig. 3.5, and when wiring up this diagram should be used in close conjunction with Fig. 3.2.

With a circuit board of this complexity it is impossible to give a point to point wiring diagram, so all the pin numbers of the integrated circuits have been given on Fig. 3.2.

The best strategy to employ when wiring up is first to label all the i.c.s with sticky labels so as to correspond to the i.c. numbers in Fig. 3.2. Wiring should be carried out using thin single core wire and wherever a number of wires need to share the same i.c. pin a terminal pin can be used to make this easier.

The circuit should be built up in blocks, checking the functioning of each block before proceeding to the next. The first block should be the clock circuit, followed by the counter (IC6), the decoder (IC5), then one digit strobe gating circuit (one gate of IC2, the corresponding gate of IC4 and its associated 20V switching circuit).

When wiring the integrated circuits it is a good idea to wire up all the power supply lines (5V and 0V) before the logic gates themselves as this allows the functioning of the i.c. to be checked as its wiring is completed.

continued on page 776

This display system developed at the Mullard Central Applications Laboratory can display up to 16 rows of 80 characters, each character being generated on a 7 × 5 dot matrix

where it is positioned until commanded to change position, and the simple deflection waveforms required are generated from the digital commands by two differential integrators which can utilise readily available operational amplifier i.c.s.

APPLICATIONS

There is a rather expensive oscilloscope on the market which uses a built in alpha-numeric character generator to write on the screen, alongside the waveform being examined, the settings of its important controls. This is a very useful feature, albeit a bit of a luxury, and using the techniques previously outlined a similar scheme could be built into a humbler oscilloscope if desired.

By substituting a "bare bones" deflection system for the oscilloscope a "built-in" display system for any type of instrument which requires to give an alpha-numeric readout could be arranged, though this would only be an economic proposition if several lines of data were to be displayed.

THE FUTURE

This series has attempted to show the variety and versatility of alpha-numeric display devices, ranging from the well-established cold cathode tubes to liquid crystal types which are still in a development stage.

An increasing proportion of the resources of the large electronics firms is being devoted to the development of cheaper and more efficient display devices since this is recognised to be an area with an immense potential market. No doubt during the time that this series has been running some new technologies have been developed.

As with all integrated circuits the price of display devices is bound to come crashing down as soon as production is really underway and there seems little doubt that the days of the electromagnetic meter are well and truly numbered! ★

P.E. DIGI-CAL

continued from page 762

Following the construction of one digit strobe circuit, the seven segment decoder (IC10) and one group of matrix diodes (corresponding to the position of the previously wired digit strobe gate) can be wired in and the single digit display tried out with dummy inputs to the SN7446.

TESTING ONE DIGIT

If this single digit operates correctly then the other digits can be connected up one at a time and tested in the same way. When all digits are wired in then all of them will display the dummy input to IC10.

Wiring up the data bus selection gates IC11, IC12 can be carried out next and these can be checked by using dummy data on either the ANSWER DATA inputs or the ENTRY DATA inputs the unwanted input being disabled by earthing its control wire.

Apart from using fixed earthing jumpers to provide the dummy inputs, it is possible to use the A, B, and C outputs of the SN7490 counter with the D input of IC10 shorted to earth. With this arrangement the displayed data counts in synchronism with the counter, the display showing 01234567. Removing the earth from the D input will give eight and nine in the first two positions of the display (the other six can be ignored) thus checking all possible inputs to the SN7446.

With the basic display system in operation the decimal point (IC8) and ripple blanking (IC9) can be added and tested.

Connections to the edge of the board were made with an edge connector socket in the prototype, but this is not necessary and connections can be made permanently via terminal pins if desired.

DIODE MATRIX

A second piece of Veroboard is used to provide the seven segment bus outputs from the decoder, this method of construction giving a very pleasing appearance and solid mechanical structure to the completed matrix.

The seemingly impossible task of lowering a piece of Veroboard down onto the protruding wires of 56 diodes all at once was eventually overcome by countersinking the holes in the Veroboard using a drill bit, thus providing a funnel which unerringly guided the wires into the correct holes.

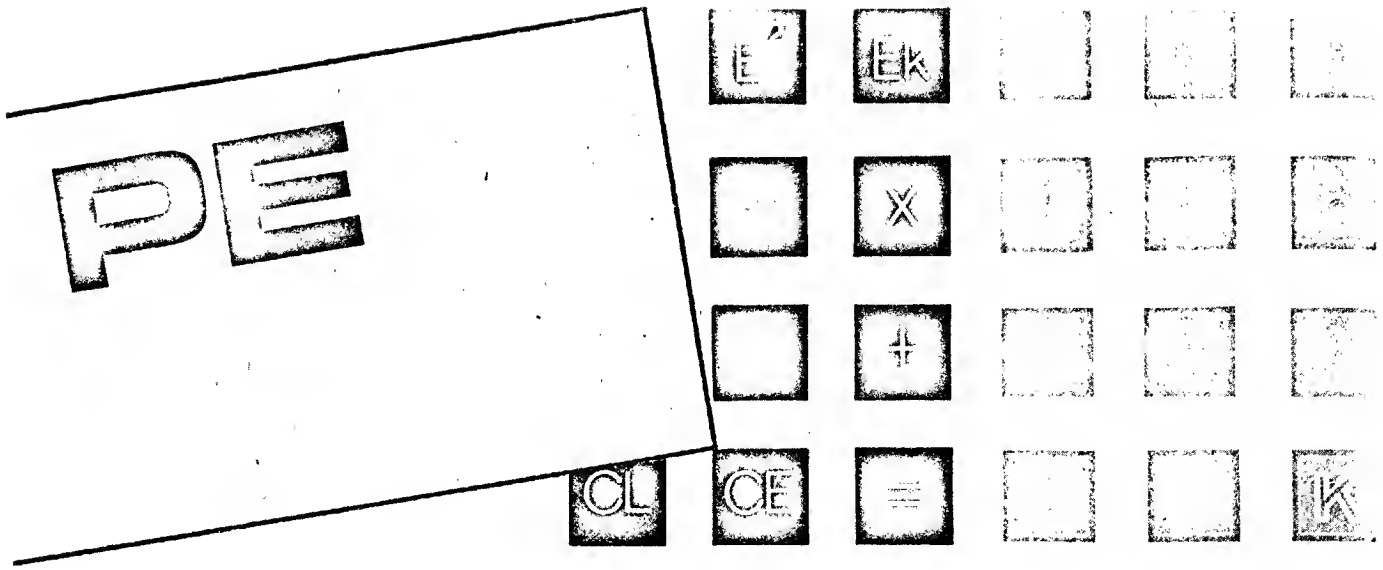
It is of course necessary to arrange the diodes in neat ranks on the mother board, and to crop their leads to about ¼in before lowering the matrix board.

VOLTAGE RATINGS

The SN7445 and SN7446 devices specified in the components list and circuit have a breakdown voltage of greater than 30V which is more than adequate for this application, but as many constructors will have noticed there are devices which are logically identical but with 15V breakdown ratings more freely available in the shape of the SN74145 and the SN7447 respectively.

The prototype employed the latter types with no ill effects, but if these types are chosen it must be realised that a certain amount of gambling is involved since you may purchase a device with one or more outputs which break down very close to the 15V minimum quoted in the specification.

Next month: Keyboard logic and hardware



By R.W.COLES PART 4

KEYBOARD LOGIC AND HARDWARE

SATISFACTORY functioning of the keyboard is vital for correct calculator operation and to make things as easy as possible for the user, a great deal of thoughtful design has been carried out as regards key-top labels, keyboard layouts, the required function of each of the keys, and compensation for possible "finger-trouble"! The author's solutions to these problems are embodied in the Digi-Cal keyboard, but should any constructor wish to alter either the physical layout or the logic there is plenty of scope for modifications to produce a "custom" design.

KEYBOARD DEFINITION

The keyboard circuitry can be split up into a number of independent or interlocking sub-circuits, and each of these performs a different function, corresponding to one of the following list of keyboard requirements:

1. Convert figure key depressions into a four bit B.C.D. code and generate a single coincident clock pulse to enter the B.C.D. data into the (separate) entry register.
2. Convert arithmetic key depressions into a static two bit code suitable for use by the programme and arithmetic sections.
3. Record the number of decimal places in each figure entry and control the final alignment of the number so that it has the correct number of decimal places as entered on the thumb-wheel switch.
4. Produce a three bit code representing the number of decimal places to be displayed, dependent upon whether entries or answers are being read out.
5. Generate a single pulse to start the programme when the EQUALS key is pressed.
6. Switch on the overflow lamp when an OVERFLOW input is received from the arithmetic section.

BLOCK DIAGRAM

The circuit of the keyboard panel can be subdivided into a number of relatively straightforward logic groups.

Fig. 4.1 shows these groups laid out in the form of a functional block diagram and it is best to understand the keyboard using this diagram before studying the full circuit in detail.

In the block diagram the circuit has been simplified as far as possible and the symbol consisting of a switch in a box with an arrowed input is used to represent gating functions which control the switched path, the arrow showing the input which has control.

ARITHMETIC KEYS

Starting at the top of the diagram, the four main arithmetic keys are fed to an encoding circuit which generates a unique binary code for each depression. This code is "staticised" in two latch flip-flops so that the code remains on the output wires until overridden by a future (different) arithmetic selection.

The E^2 key is in parallel with the "MULTIPLY" key since squaring is simply a modified multiplication sequence; a separate E^2 output is also produced to modify the programme.

The narrow START pulse required by the programme is generated by a monostable triggered by the EQUALS key, and this monostable is also used to start the second half of the multiply and divide sequences on command from the arithmetic section.

NUMERAL KEYS

The number keys are encoded to their B.C.D. equivalent in a diode matrix, the outputs of which are also staticised by four flip-flops so as to present a steady logic output during the clock pulse which enters the data into the entry register, the data in the latches remaining until either a different number key is pressed, or the EQUALS key is pressed in which

KEYBOARD LOGIC

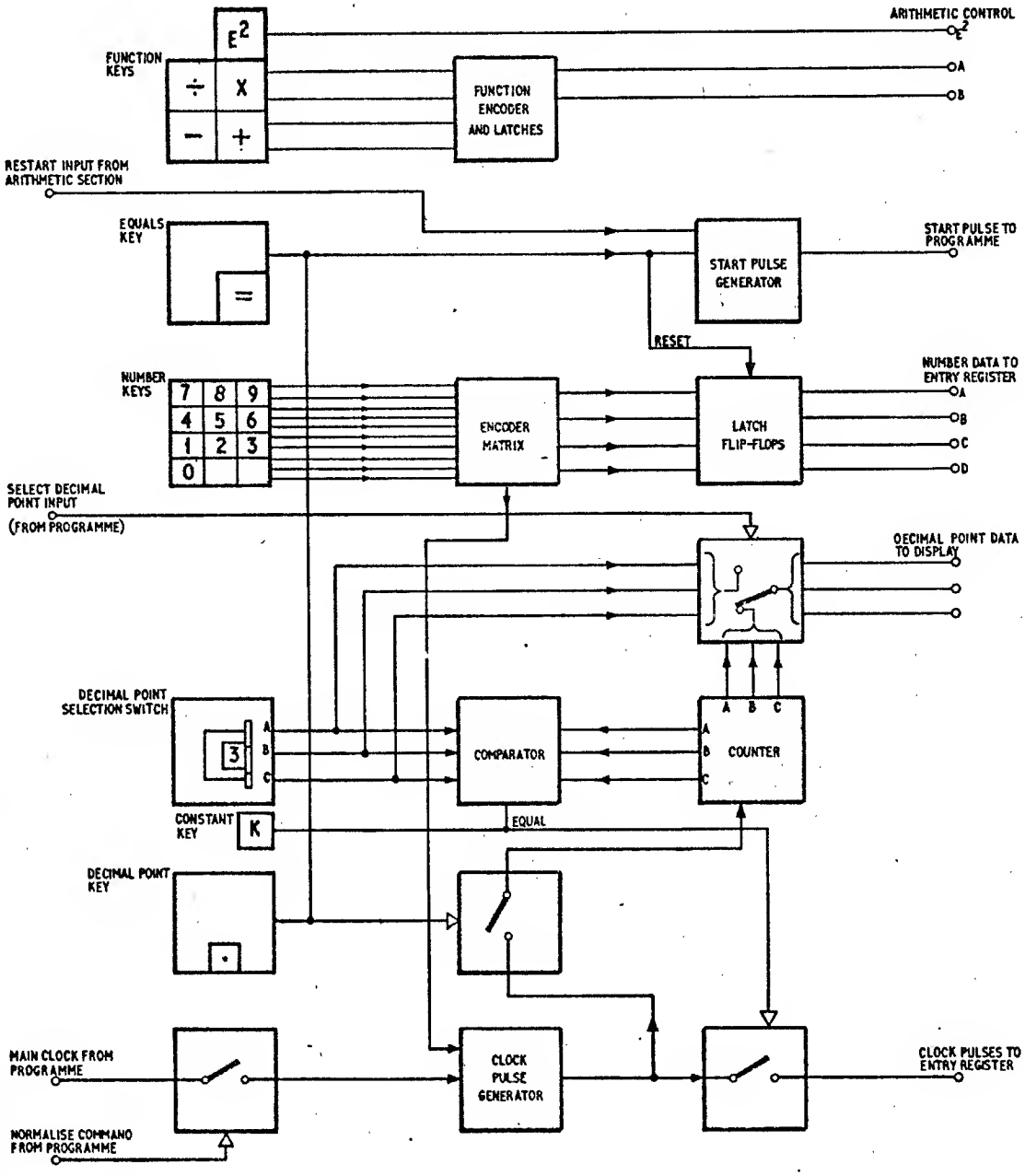


Fig. 4.1. Simplified block diagram of the keyboard logic. The symbol of a switch in a box with an arrowed input represents a group of logic gates, the arrow being the input which has control

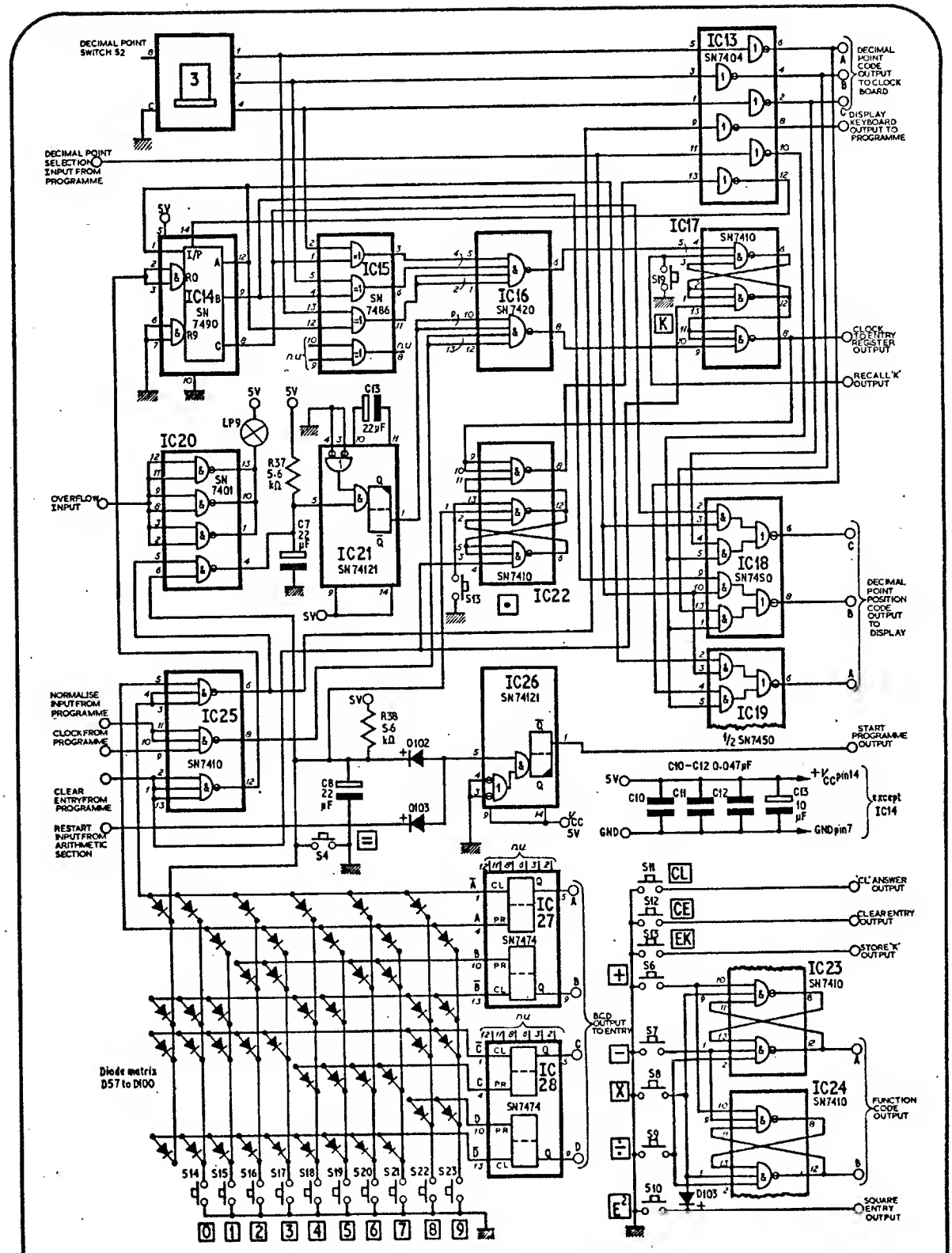


Fig. 4.2. The complete circuit diagram of the keyboard logic panel. All i.c.s have pin 7 as ground and pin 14 as 5V except IC14 whose power supplies are shown

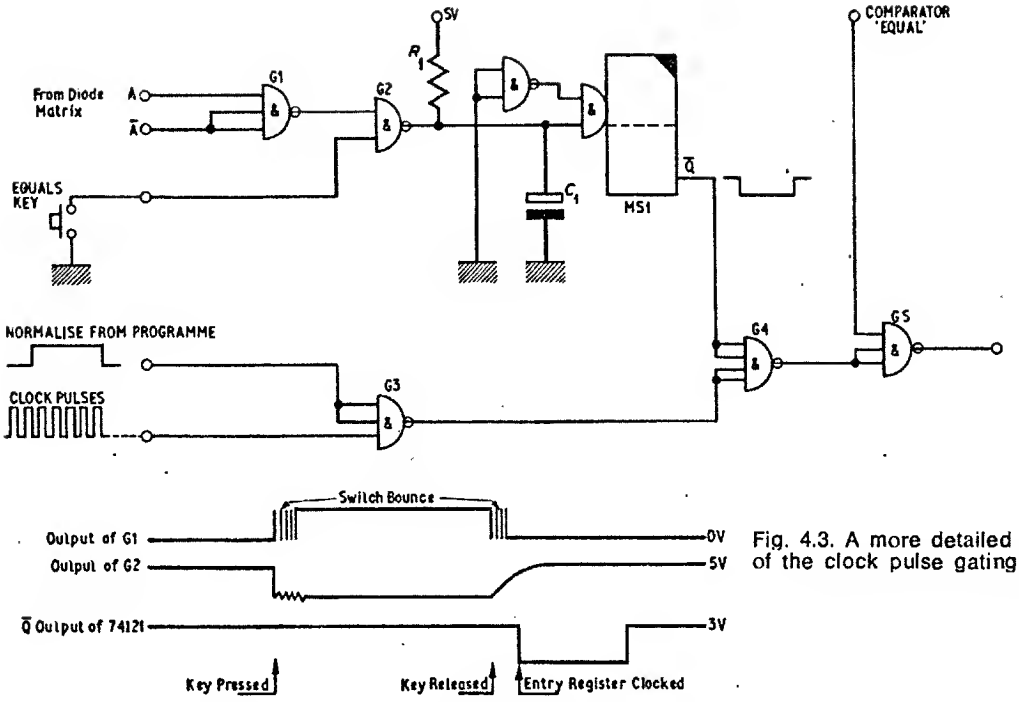


Fig. 4.3. A more detailed diagram of the clock pulse gating circuit

case the latches are cleared. An output is also generated from the matrix whenever any key is pressed, and this signal is used to trigger the clock pulse generator, but more of this later.

DECIMAL POINT POSITIONING

If the decimal point key is pressed during an entry then a latch is set which in turn opens a gate to allow any subsequent clock pulses through to a counter. This counter counts the clock pulses after the point entry and gives an output which is compared with the setting of the decimal point thumbwheel in a comparator circuit.

When the correct number of decimal places have been entered the comparator registers the equality and shuts off the clock pulses from the clock pulse generator. It is this mechanism which prevents entry of too many decimal places in any figure entry.

If the number entered has too few decimal places then when the programme is started a NORMALISE command from the programme allows the main calculator clock pulses through to the clock generator in the keyboard, and the entry register data is rapidly shifted along until the comparator again registers equality then shuts off the clock.

This process ensures that all numbers can be entered without regard to the position of the point, normalisation being automatically carried out by the calculator itself.

OTHER FUNCTIONS

There are two additions to the clocking circuit to allow for special conditions. The EQUALS key is allowed to close the path connecting the clock pulses to the counter, this being done to cater for the occasions when only whole numbers are entered, the decimal point being unused.

Also, the RECALL CONSTANT (K) key is allowed to shut off the clock path to the entry register so as to inhibit normalisation, this being necessary because the constant in store is correctly aligned to start with.

The three bit output of the thumbwheel switch is used to define decimal point position when the answer to a calculation is being displayed, and the three bit output of the counter is used to define it when an entry is being displayed. Switching between the two sources is carried out by a gating arrangement controlled primarily by the programme.

Any keys not shown on the simplified diagram have no associated logic circuitry and are passed out to the rest of Digi-Cal as switch closures to earth.

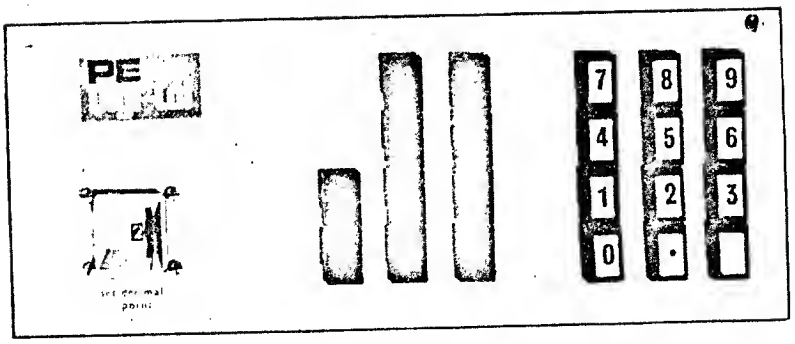
The full circuit of the keyboard is given in Fig. 4.2, and with the knowledge of its operation gained from the simplified diagram it should be possible to pick out the various logic groups previously discussed. One particular group may still be a little difficult to trace out, and that is the clock generation and gating.

To see this circuit in a clearer light it has been redrawn in Fig. 4.3 in an integrated way, and because this section is so important we can go through it step by step.

CLOCK CIRCUIT

The clocking is initiated by detecting any output from the diode matrix which is an indication of a key depression. Because the normally high A, B, C, and D outputs of the matrix will always have either their true or their complement output active (i.e. low) for any one of the ten relevant key depressions a detection circuit can be made by "ORing" together the true and complement version of any one of them.

In Fig. 4.3 G1 performs the detection by using the two "A" outputs from the matrix. The "logic 1"



The upper side of the keyboard showing the arrangement of the switches in the slots

output from G1 is applied to G2 which is an open collector gate with R_1 and C_1 in its collector circuit to give a slow "0" to "1" transition. The other input to G2 is an inhibiting input from the EQUALS key which prevents a clock pulse being generated by the latch reset when the EQUALS key is pressed.

The output of G1 is shown for a typical key depression and as you can see it carries with it a faithful (though inverted) representation of the switch bounce which is a feature of all mechanical switch operations, and which must be removed before the signal is used to trigger the monostable.

The output of G2 is "cleaned-up" by R_1 and C_1 to give the output pulse shown, and the slow transition after the key is released is used to activate the level sensitive trigger input of the SN74121. The fairly long negative going pulse from the monostable is "ORed" with the possible output of G3 and fed out to the entry register via G5 which is controlled by an inhibitory input from the COMPARATOR EQUAL latch. Gate G3 is used to control the main clock input used during the normalising cycle, being enabled by a long pulse from the programme.

DIODE MATRIX

The diode matrix used to encode the figure keys into their binary equivalent is so named because of its physical construction, the logic it performs being simply that of eight multi-input OR gates, the number of inputs to each gate being set by the number of diodes connected to its output line.

In the circuit diagram the eight horizontal lines represent the gate outputs, the requisite inputs being made by the diode links to the eleven vertical lines from the number keys and the reset line.

The matrix is built using the same technique as was employed for the display matrix (Part 3) with a small piece of Veroboard providing the vertical output lines to the latches and the key inputs being wired to the horizontal strips on the mother board.

Remember that it is necessary to make guide funnels on the blank side of the small piece of Veroboard to ease the location of the diodes prewired to the mother board, and most important, the cathode end of the diodes should be mounted next to the mother board.

The outputs from the matrix drive the PRESET and CLEAR inputs of the four latch bistables, which do not use their D inputs or CLOCK inputs in this application (IC27, IC28).

The use of SN7474 flip-flops in this position is a bit extravagant, since a couple of SN7400s cross coupled to form four latches would work just as well and can be incorporated if desired, the more versatile SN7474s being used in the prototype to allow for possible future modification to enter data automatically from a source such as a tape reader.

FUNCTION CODER

Unlike the number coder and latches, the function coder and latches do not need a separate set of coding gates, the latches being built from SN7410 three input NAND gates, ICs 23 and 24, and the two inputs to each gate left after making the latch coupling are sufficient to provide the gating required to encode the arithmetic keys.

The E^2 key is coded in the same way as MULTIPLY and a diode D103 is used to facilitate this.

EQUALS KEY

Pressing the EQUALS key is the signal to start the selected arithmetic programme, and as may be expected, when it is pressed several things happen at once.

The earth appearing on the EQUALS line:

(a) resets the number latches via the matrix;

(b) inhibits the generation of a clock pulse which would normally result from the previous reset (see G2, Fig. 4.3);

(c) sets the decimal point latch IC22 to allow subsequent clock pulses through to the counter (this latch may have already been set by operation of the DECIMAL POINT key during figure entry).

When the key is released and the earth disappears the resulting positive going signal on the line is "debounced" and used to trigger the START PROGRAMME monostable IC26 via a simple diode gate D101, D102. The output from the monostable is a very narrow pulse which is used to initiate the programme sequence. The diode gate is required so that the programme can also trigger the monostable to generate a "RESTART" pulse required in some arithmetic sequences.

DECIMAL POINT NORMALISATION

When the decimal point latch is set clock pulses are allowed through to the SN7490 decade counter IC14, which in effect counts the number of figures after the point in a number entry. The contents of this counter are continually compared with the decimal point switch output so as to detect a state of equality.

The thumbwheel switch output is already in a binary code though of an inverted form so that a logic "1" is represented by an earth connection and

COMPONENTS . . .

KEYBOARD PANEL

Resistors
R37, R38 5·6kΩ ¼W ±10% carbon

Integrated Circuits

IC13	SN7404
IC14	SN7490
IC15	SN7486
IC16	SN7420
IC17	SN7410
IC18, IC19	SN7450 (*or* SN7451) (2 off)
IC20	SN7401
IC21	SN74121
IC22, 23, 24, 25	SN7410 (4 off)
IC26	SN74121
IC27, IC28	SN7474 (2 off)

Diodes
D57–D103 West Hyde type "red" (47 off)

Capacitors
C7, C9 22μF 15V elect. (2 off)
C8, C13 10μF 15V elect. (2 off)
C10, C11, C12 0·047μF (3 off)

Switches
S2 Birch Stolec EB10N 1248 and a pair of end plates
S3-S23 On/off push button (Bulgin type MP22, white 12 off, black 9 off)

Lamp and holder
LP9 6V 40mA lamp and holder (Bulgin type D22)

Miscellaneous
9·5in×3·3in 0·1in matrix Veroboard

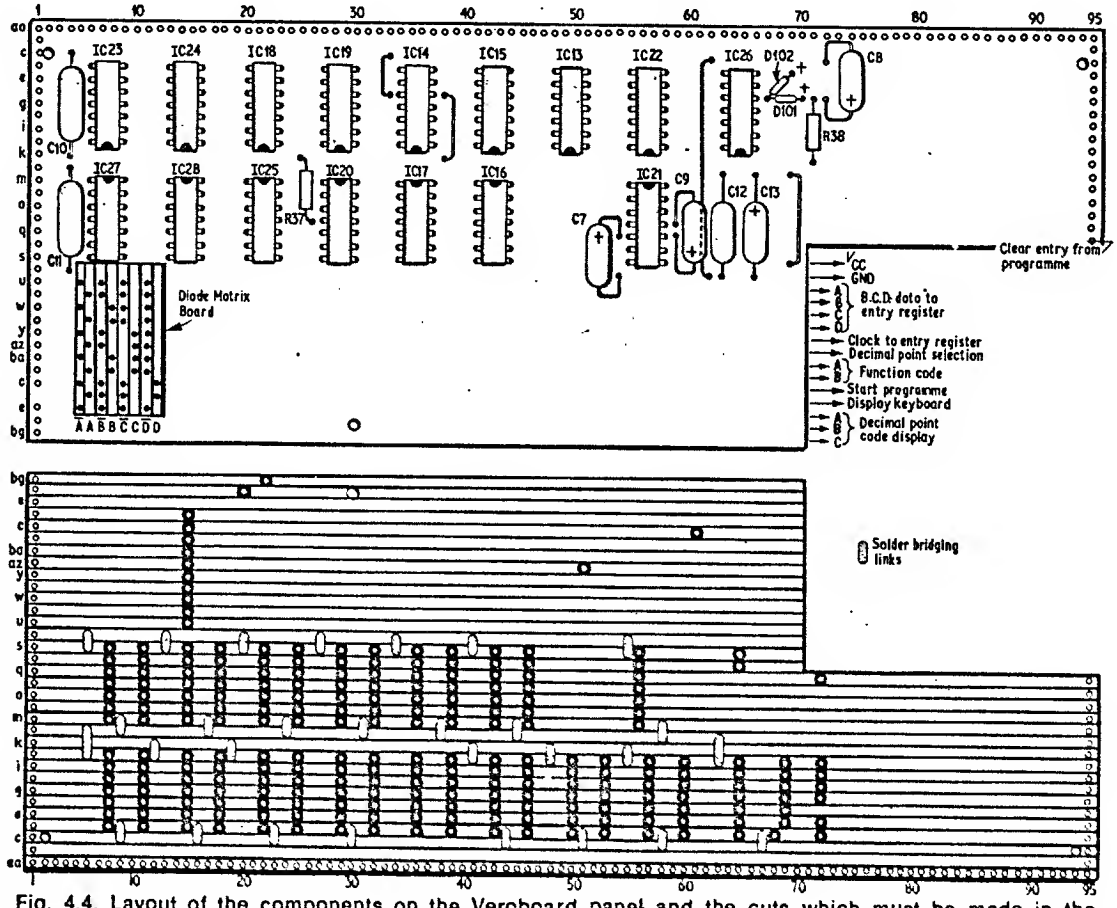
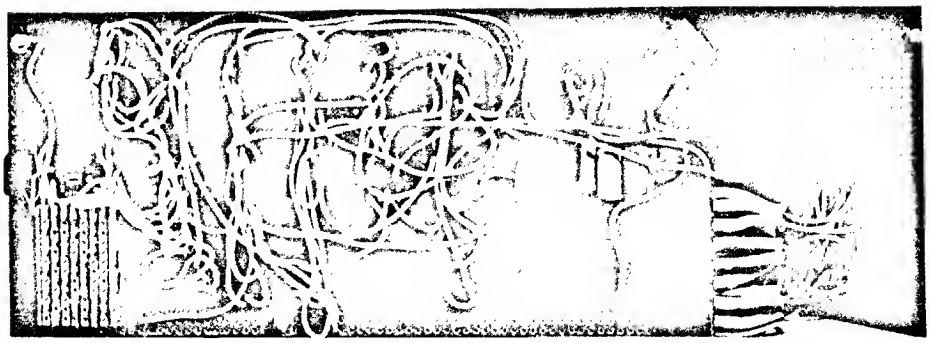


Fig. 4.4. Layout of the components on the Veroboard panel and the cuts which must be made in the copper strips. The links shown are for the power supply lines only and can either be made above or below the board. The black dots on the "diode matrix" board show the positions of the diodes which are arranged with the cathodes towards the main panel



A photograph of the keyboard logic panel in the prototype. The edge connector is an optional extra as wires can be soldered directly to the board

logic "0" by an open circuit. This suits our purpose admirably since the SN7486 used as a comparator, IC15, gives a "1"" from each of its gates when its inputs are exactly opposite.

By comparing the true counter outputs with the complement switch outputs a comparator is formed which gives three "1" outputs when the count equals the switch setting. These three ones are used to enable a gate IC16, which in turn sets a latch, IC17, the output of which forms the input to G5 of Fig. 4.3 and serves to shut off the supply of clock pulses to the entry register.

DISPLAY CONNECTIONS

The position of the decimal point in the display can be governed either by the contents of the counter, IC14, or by the thumbwheel switch setting depending on a command from the programme.

Switching between these two sources is carried out by the AND OR INVERT gates IC18 and IC19, but note that for this purpose the outputs from the thumbwheel switch are inverted by IC13, to make them compatible with the counter outputs. The selected point data is fed to the display via a three line bus.

OVERFLOW INDICATION

If an OVERFLOW condition is detected during an arithmetic operation a "1" input on the OVERFLOW line drives three SN7401, IC20, gates in parallel to switch on the panel indicator bulb. The correct procedure is then to use the CLEAR key to erase all data and then re-enter the problem in a rescaled form. It is necessary to parallel connect three gates for this job because of the current requirements of the bulb.

PROGRAMME RESET

To return the keyboard to its correct state for a further calculation it is necessary to rest the DECIMAL POINT and EQUALS latches and the decimal point position counter. This is carried out by a CLEAR ENTRY command from the programme which, as its name implies, also clears the contents of the entry register.

CONSTRUCTION

The layout of the Veroboard panel is shown in Fig. 4.4, the panel itself being cut to size from a West Hyde type 122 board.

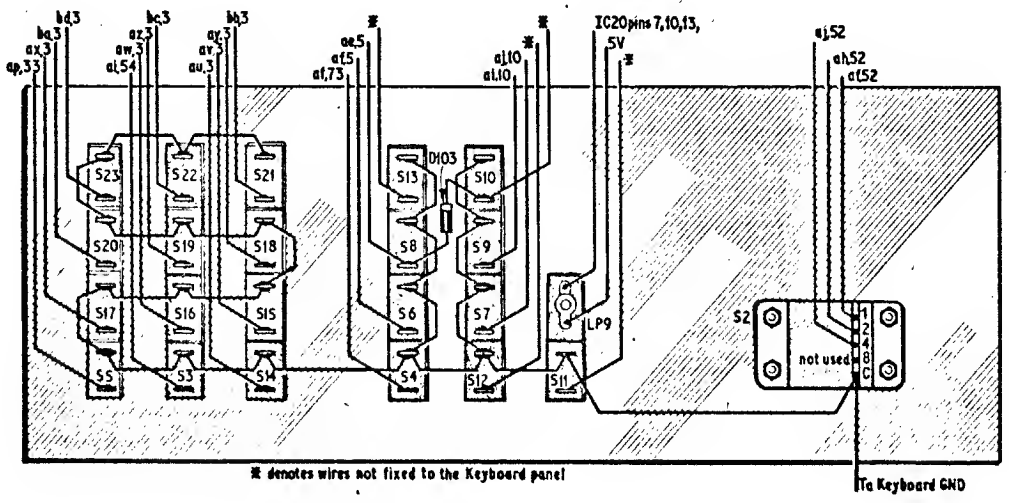


Fig. 4.5. The switches are wired as shown. All wires except those with an asterisk go to the panel shown in Fig. 4.4

The finished panel will be mounted upside down under the keyboard proper, affixed to the recessed wooden blocks either by means of wood screws, or, as in the prototype, by captive 6B.A. bolts cemented into the blocks with Araldite.

Needless to say, it is advisable to make all the board fixing arrangements before commencing the wiring.

Wiring up is carried out as before with thin single core wire, using terminal pins where necessary to increase the wire handling capacity of a particular pad.

Off board wiring is achieved with thin flexible stranded wire left long enough that the board can be easily removed for access, but not too long that stray pick-up could become a problem.

An edge connector was used to carry some of the off-board wiring in the prototype to help with development, this would not be necessary, or even advantageous to any significant extent with later versions, due to the very large number of interconnections required in all.

The switches are wired up as shown in Fig. 4.5.

TESTING

As with the display board last month it is advisable to wire up the keyboard logic a section at a time, testing each block before proceeding. In this way small mistakes can be easily discovered and dealt with before they become buried in several different circuit blocks.

Almost all the logic can be tested at the wiring stage without undue complication, outputs being monitored with a multimeter or by connecting them temporarily to the display board input if desired. If the latter course is chosen remember that the display board requires an inverted B.C.D. input, which while easily accommodating the decimal point outputs and function code outputs, will require temporary connection to the $\overline{Q}$ rather than the Q outputs of the figure latches for correct display.

The clock pulse output is long enough to be detected on a meter which is an advantage for tests of this type, the EQUALS triggered START pulse is however far too short to be detected in this way but fortunately this part of the circuit is quite simple and can be left unchecked at this stage.

Next month: Entry Register (constant store, entry register and multiplexer)

POINTS ARISING

SQUARE WAVE GENERATOR *(Sept. 1972)*

In the lower half of Fig. 6, the connections for the switch should read as follows reading from top to bottom:
(a) Top group is S1b numbered 1,2,3,W,4;
(b) Bottom group is S1a numbered 4,3,2,1;
(c) S1b wiper should read S1a wiper.

NEWS BRIEFS

TECHNICAL INFORMATION SERVICE

A NEW technical information service, aimed at giving firms, corporate bodies, instructors, students, and others engaged in educational work, advice on correct electrical installation practice according to I.E.E. "Regulations" has been established by the National Inspection Council for Electrical Installation Contracting.

The service is confined to technical matters and excludes advice on commercial or trading aspects, industrial or labour relations, and information relating to manufacturers' products.

The aim is to promote a high standard of installation and maintenance safety of electrical wiring and appliances. The subscription fee is £3·50 per year to cover the services offered. Further information is available from the Council at Trafalgar Buildings, 1 Charing Cross Road, London SW1A 2DT.

NEW POCKET CALCULATOR

WHAT is claimed to be the world's smallest electronic calculator has just been announced by the British company Sinclair Radionics Ltd. At only just over ¼in thick and 5½in × 2in this can really claim to be a pocket sized calculator.

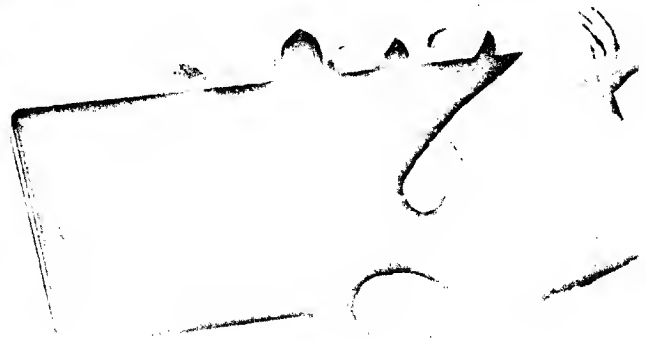
Known as the Sinclair Executive this calculator embodies many new techniques. Firstly the single MOS chip which forms the calculator consumes a mere 20 mW of power making it possible to run the whole machine from three mercury cells of the type used in hearing aids. This is made possible by switching off the i.c. completely between clock pulses relying on the capacitance of the MOS elements to store the information. Secondly the clock rate is reduced when the calculator is not performing a calculation so as to conserve power.

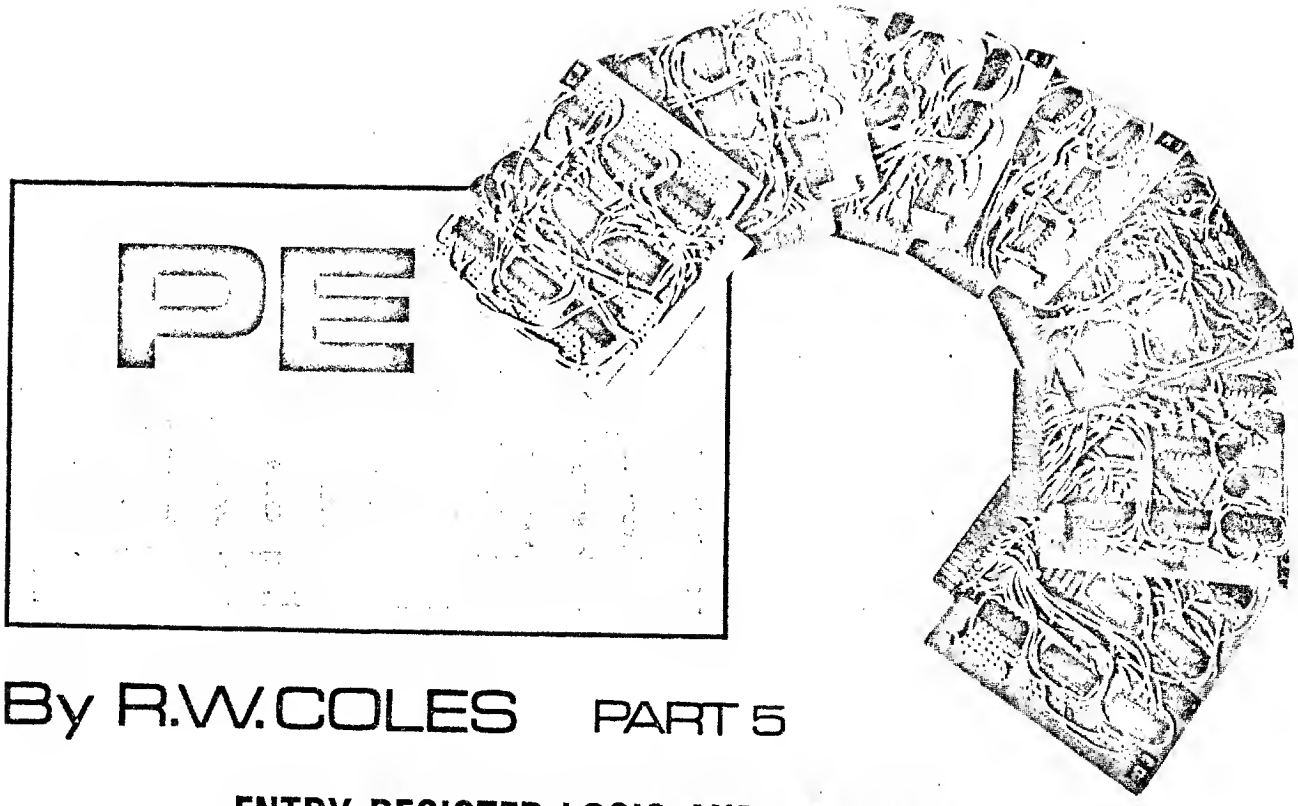
The battery voltage is just sufficient to drive the display thus eliminating the usual dropper resistors which consume power.

The keyboard was specially developed for the calculator being only 4mm in depth. The contacts are gold plated and the keys are arranged so that it is virtually impossible to touch two at the same time.

The L.E.D. display has a capacity of eight digits. The calculator can perform all the usual arithmetic functions as well as automatic squaring, reciprocals and can operate in either fixed or floating decimal point mode. It also has a memory for calculations with a predetermined factor.

Although, at £79 this calculator is not the cheapest on the market, it must pose quite a threat to the present Japanese domination of the calculator field.





By R.W.COLES PART 5

ENTRY REGISTER LOGIC AND HARDWARE

LAST month we dealt with the construction of the keyboard logic panel which has the function of converting each key depression into suitable logic signals for entry and control of data.

As stated in the first part, entries of up to six digits can be made. The subject of this month's part is the Entry register and associated logic which has the function of storing these six entered digits in their correct order for use in calculation to come. A six digit number can also be placed in a memory for use at any number of times during the calculation.

This part also discusses the possibility of a "fixed constant" key whereby a single depression of an extra key causes a chosen number (such as π) to be entered into the entry register.

ENTRY REGISTER LOGIC

A block diagram of the ENTRY register complex is shown in Fig. 5.1, which is an expansion of the ENTRY register section of the overall arithmetic section block diagram from Part 1 (Fig. 1.3).

The operation of the ENTRY register and its associated constant store and display multiplexer is relatively straightforward, each of the possible six decimal entry figures being stored as a four-bit parallel B.C.D. code, requiring a total of 6 × 4 (= 24) separate storage bistables.

The 24 bistables or flip-flops are arranged as a shift register six decimal digits long and four B.C.D. digits wide, so that with each clock pulse a complete B.C.D. group (i.e. one decimal digit) is shifted into, or down, the register.

Each time a number key is pressed, the keyboard circuits (which were described last month) staticise the corresponding B.C.D. code and generate a single clock pulse, which is used to clock the four bit code into the ENTRY register.

Pressing a second or subsequent number key causes the first group to shift down the register to the "left," its place being taken by the new entry. This process can continue until the first entered number ends up in the extreme left-hand location of the register, after which any further entries will cause that first number to be destroyed by being shifted out of the end of the register.

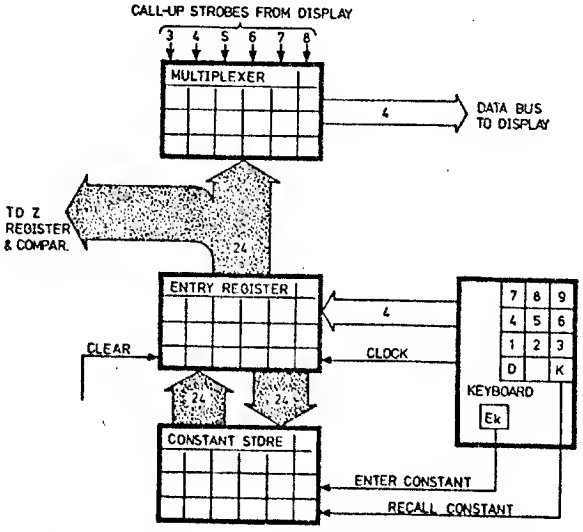


Fig. 5.1. Block diagram of the Entry Register complex showing the inputs and outputs

Note that the ENTRY register accepts the most significant digit of the complete figure entry *first*, just as we write figures ourselves. This makes the ENTRY register a "left-shift" register and distinguishes it from the other registers which normally accept the least significant digit (L.S.D.) first, and are thus termed "right-shift" registers.

CIRCUIT PARTITIONING

The ENTRY register and associated constant store and multiplexer, are built on three separate plug-in cards. The way in which the circuit is divided among the four cards is shown in Fig. 5.2., where it is immediately apparent that three of the cards are identical.

In effect partitioning the circuit in this way results in three independent shift-registers, each two decimal digits long and four B.C.D. digits wide, and each having a proportionate amount of constant storage.

In use these small units are connected in series, via the edge connector wiring, but because each card is identical they can be freely interchanged and this is a great help in tracing any faults which may occur.

The display multiplexer is built on a separate card with a 44-way edge contact instead of the 22-way type used for the other three cards, and although not shown on the block diagram, this card also houses two SN7440 buffer gate packages used to drive the CLOCK and CLEAR lines of the register.

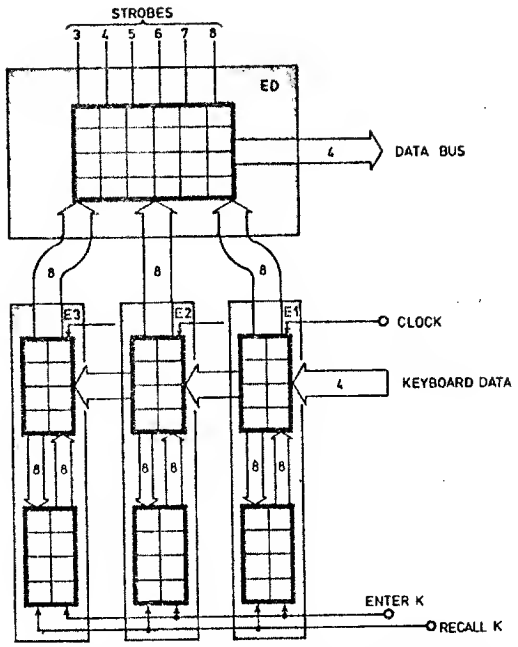


Fig. 5.2. Partitioning of the entry Register onto the four boards. Boards E1, E2, E3 are identical and each contain two digits of the entry and two digits of the stored constant. Board ED contains the multiplexer

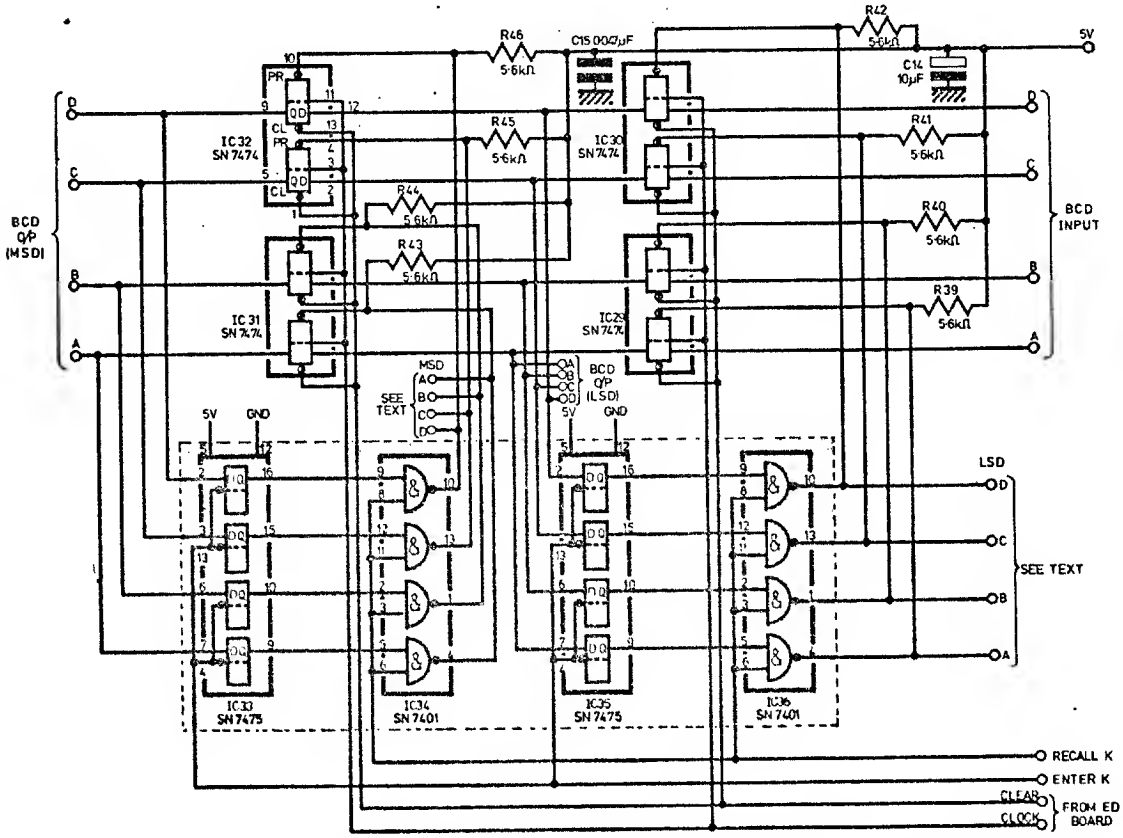


Fig. 5.3. Circuit of the Entry Register board E1. Boards E2 and E3 are identical to this. The dotted line encloses the constant store which may be omitted if not needed

REGISTER CIRCUIT

The full circuit diagram of an individual register board is shown in Fig. 5.3, three of these sections being required to form the complete register.

The circuit splits horizontally into two logical sections, the upper four i.c.s forming the shift register proper, and the lower four forming the constant store.

The components forming the constant store are enclosed in a dotted box for easy identification, and it is these i.c.s which may be left out if required, along with their associated wiring.

The eight bistables which comprise the shift register itself are SN7474 dual D-type elements, chosen because of their flexibility and low power dissipation.

Both of the two bistables in each package have independent clock, data, preset and clear inputs, together with true and inverted outputs. D-type flip-flops are more suitable than the J-K types for shift register application because they only require a single data (D) input which has the effect of reducing wire interconnections and leaving pins available for the independent preset function without recourse to the more expensive 16-pin package.

To form the register the flip-flops are connected in series pairs, there being four such pairs on each board to cater for the four separate digits (A, B, C, D) of the B.C.D. code.

Each vertical group will contain four binary digits which, taken together, represent one of the decimal numbers zero to nine.

The clock input to the register has to drive all of the flip-flop clock inputs in parallel so that after each pulse the data in a particular four bit group move one place to the left, and are themselves replaced by new data.

It is necessary to clear all the data from the ENTRY register simultaneously when required by the programme, and to this end all the CLEAR inputs are connected together to a common input, a low level, or "ground" condition on this input will set the Q outputs of all the flip-flops to zero, and the $\overline{Q}$ outputs to one.

CLEARING OPERATION

The contents of the ENTRY register are transferred in parallel to the z register early in the arithmetic programme, except during MULTIPLY, when they remain to be compared with the contents of the counter.

When the register contents are finished with the ENTRY register is cleared by a signal from the programme, ready for subsequent entries to be made by the operator.

Any errors made during figure entry (e.g. pressing "8" instead of "6") can be corrected by pressing the CLEAR ENTRY key which also has the effect of clearing the contents of the register ready for new data.

CONSTANT STORE

The constant store is shown beneath the ENTRY register, and is of the same 24 position capacity, so that any entry made can be stored for further use in a calculation.

This store is not essential to the correct operation of Digi-Cal and can be left out permanently or temporarily if desired, without the need for any modification to the rest of the circuit.

In operation, with the desired constant entered in the usual way into the ENTRY register, the ENTER K (EK) key is pressed, which duplicates the contents of the ENTRY register in the constant store by means of a single, parallel, 24 bit transfer.

Constants stored in this way remain available until they are either replaced by a new number or the machine is switched off, there being no requirement or provision for clearing this store, other than by entering a constant which consists of all zeros.

Constant recall is carried out by pressing the K key in the numeral section of the keyboard whereupon a reverse transfer occurs, in parallel, from the constant store to the ENTRY register. This operation does not destroy the contents of the store so that any constant can be used as many times as required in a calculation.

The constant store need not be used simply for storing constants in the accepted sense, since it will act as a memory of any result or intermediate answer if required, provided these numbers are entered through the keyboard in the usual way.

This mode of operation really acts as a substitute for pencil and paper, and can be most useful at times in long calculations.

DISPLAY MULTIPLEXER

The display board, described in Part 3, will display either entries or answers depending on a signal from the programme, entry and answer data being routed to the display via two four-line "buses."

Timing signals, in the shape of "character call-up" strobes are produced by the display board to enable the four line buses to carry all the data in their associated register to the display in a time-shared sequence, the sequence being produced in a multiplexer circuit.

There are two multiplexers in Digi-Cal, one for the eight digit answer and the other, which we are interested in here, to handle the six digit entries.

Only strobes three to eight inclusive are used by the ENTRY multiplexer, each of these allowing only one four-bit B.C.D. digit on to the bus at any instant in time, the strobe direction being from most to least significant digit (M.S.D. to L.S.D.).

CONSTANT CIRCUIT

Simpler storage elements can be used for the constant store since there is no requirement for PRESET or CLEAR inputs, and the devices chosen to fulfil this function are the SN7475 four bit latches.

Like the SN7474s these quad latches require only single "D" inputs, the data to be stored being of course the outputs from the shift register flip-flops.

Clocking is controlled by the ENTER K key, via a buffer gate mounted off the board. There is no need to "debounce" the output of this switch because of the simple "gated latch" operation of the SN7475 flip-flops and the static nature of the inputs during the entry operation.

Stored constants are returned to the shift register via the SN7474 PRESET inputs, transfer being controlled by the SN7401 quad NAND gates, which have a common input enabled by the RECALL K key, via a buffer gate. The PRESET inputs of the SN7474s are "active low," i.e. they set the Q output to "1" when an "0" input is present, and so require inverted data from the constant store. This inversion is provided by the SN7401 gates.

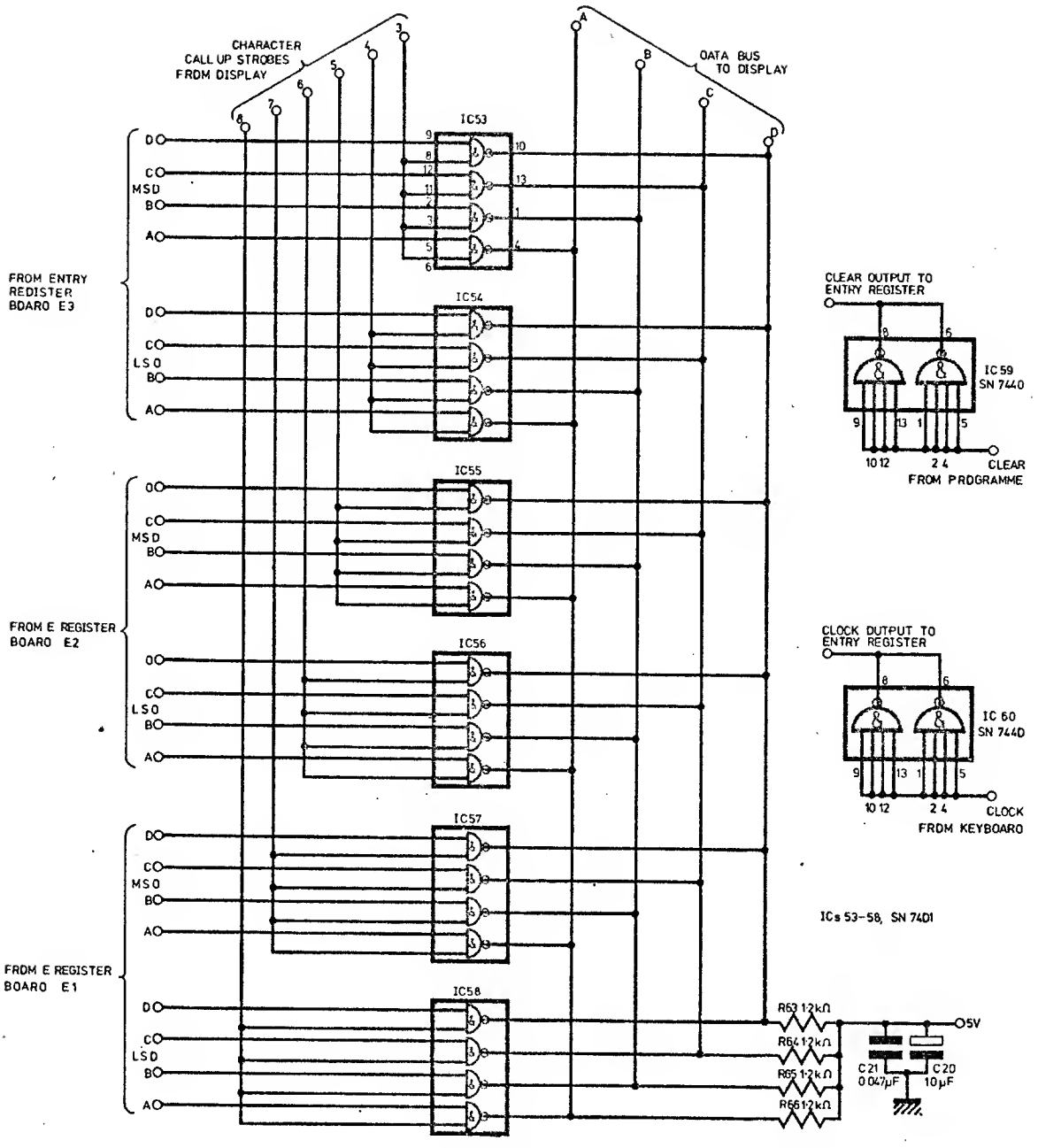


Fig. 5.4. Circuit of the Entry Register Board ED. The two SN7440 i.c.s are simply buffers and only placed on this board for convenience

MULTIPLEXER CIRCUIT

The circuit of the display multiplexer, Fig. 5.4, is quite straightforward, it being formed only from gates and resistors. Each SN7401 gate package has its four inputs wired to the corresponding four B.C.D. output pins on the appropriate register board, there being a separate gate i.c. for each decimal digit.

The common input to the four gates in each i.c. is driven by the "character call-up" strobe appropriate to that digit.

All the "A" outputs from the gate packages are wired together, as are the B, C, and D outputs, to form the four line display bus, which is referenced to the 5V line by the four 1·2 kilohm resistors.

Note that SN7401 open collector gates are essential for this circuit, SN7400 gates being unsuitable due to the fact that several gate outputs are connected directly together to provide the "Wired OR" function.

Interconnection of outputs is not permitted with the basic TTL gate because of the "active pull-up"

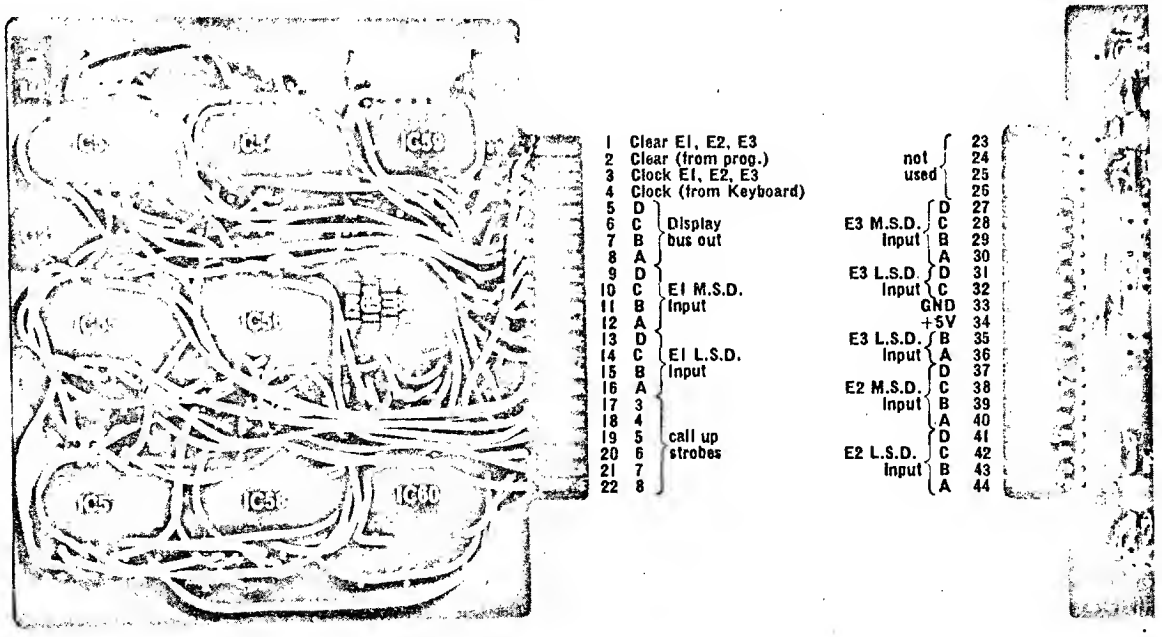


Fig. 5.5. Layouts of the components on the register board ED and functions of edge contacts

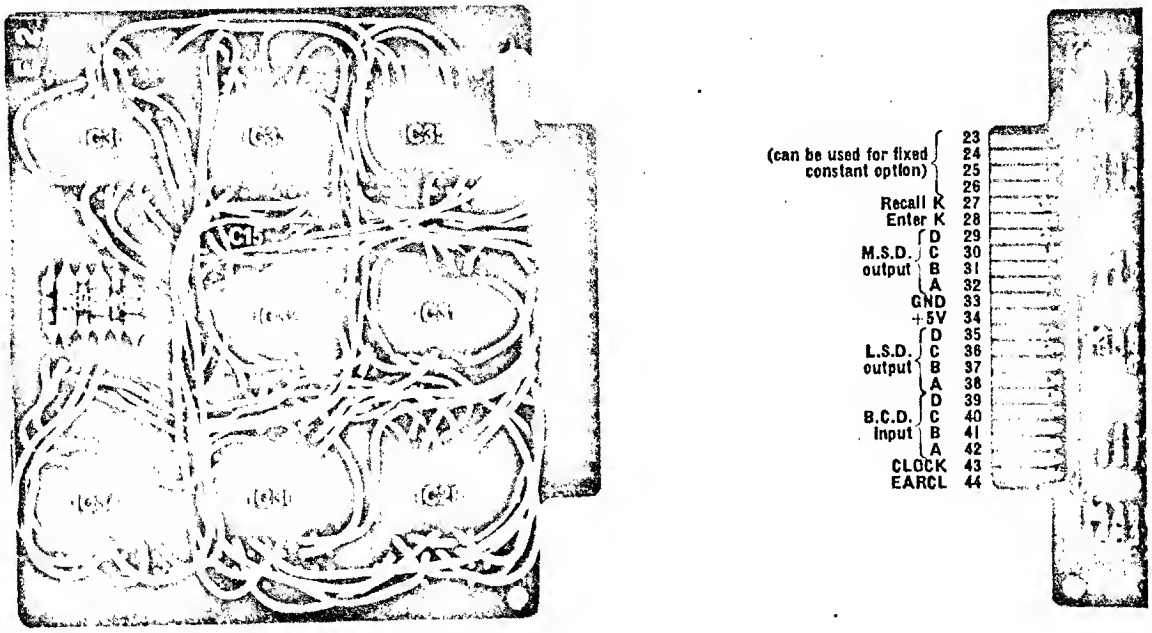


Fig. 5.6. Layout of the components on the Entry Register Boards E1, E2, and E3 and functions of edge contacts which only appear on the underside

COMPONENTS

REGISTER BOARDS E1, E2, E3

Resistors
R39–R62 5·6kΩ ±10% ¼W carbon (24 off)

Capacitors
C14, C16, C18 10μF 15V elect. (3 off)
C15, C17, C19 0·047μF (3 off)

Integrated Circuits
IC29–IC32, IC37–IC40, IC45–IC48 SN7474 (12 off)
IC33, 35, 41, 43, 49, 51 SN7475 (6 off)
IC34, 36, 42, 44, 50, 52 SN7401 (6 off)

Printed circuit boards and sockets
Type DL109/22 (3 off) (Available from Shirehall Electronics Ltd., Station Yd., Borough Gn., Sevenoaks, Kent)
SK2–4 DPK165 edge connectors (Shirehall) (3 off)

(Note that the three boards are identical, each board taking one third of each group of components shown above)

REGISTER BOARD ED

Resistors
R63–R66 1·2kΩ ± 10% ¼W carbon (4 off)

Capacitors
C20 10μF 15V elect.
C21 0·047μF

Integrated Circuits
IC53–IC58 SN7401 (6 off)
IC59, IC60 SN7440 (2 off)

Printed circuit board and socket
Type DL109/44 (Shirehall)
SK1 DPK165 edge connector (Shirehall)

output stage. The SN7401 is a gate specially produced to allow "Wired OR" function in TTL systems, and has no pull-up device incorporated.

The two SN7440 buffer gates are positioned on the multiplexer board but have no direct connection with the multiplexer circuit. The two buffers in each package are wired in parallel to give sufficient drive capability (or "fan-out") to handle the large load represented by the ENTRY register CLOCK and CLEAR lines (48 loads and 72 loads respectively).

CONSTRUCTION

Wiring up is carried out in the same fashion as the display board described last month, though the plug-in cards are much easier to work with because of the pre-tinned finish and the ready formed i.c. pads which obviate the need for "spot face" cuts.

By referring to the appropriate circuit diagram and the i.c. layouts shown in Fig. 5.5 and Fig. 5.6 wiring is quite straightforward, the only points to remember being the need for links from the power buses to each i.c. and from these power buses to the appropriate edge contacts, along with the need to orientate the i.c.s correctly before soldering into circuit.

All wiring up is carried out on the blank side of the boards, using single core wire.

The best order to complete the construction of the boards is as follows: ED board (display multiplexer) including the buffer gates, on a Shirehall DL109/44; then the register section (SN7474s) of boards E1, 2, 3, on Shirehall DL109/22 cards; and finally when the above sections are operating correctly, the constant store and if required, the fixed constant option, may be added.

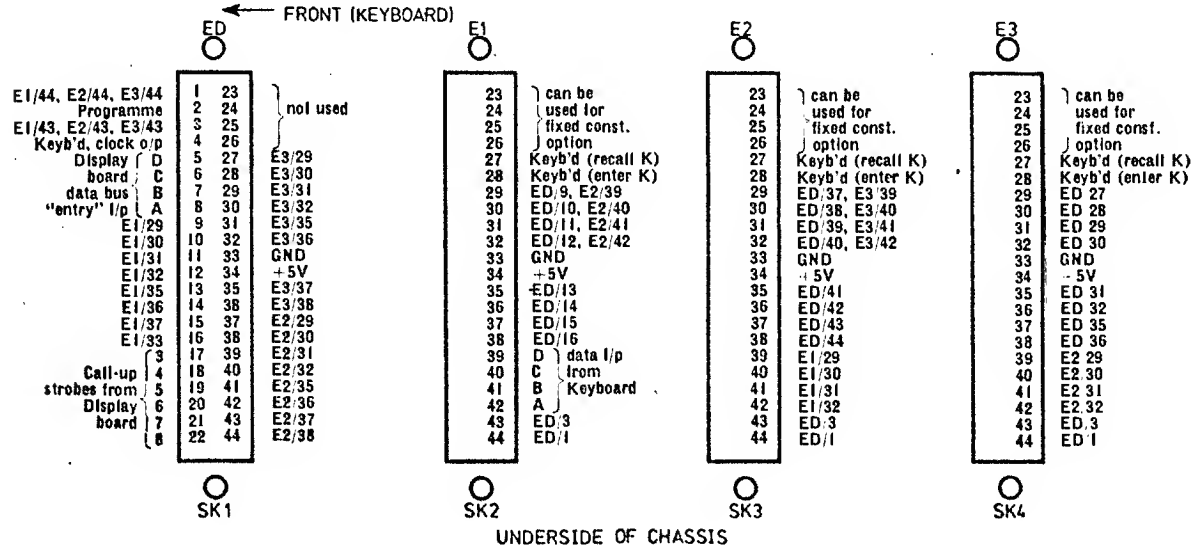


Fig. 5.7. Interwiring of the four entry register boards is carried out using the edge connectors fitted in the large hole cut in the chassis plate. The edge connectors are fitted so that the boards plug in from above. Destinations of wires are shown next to each contact (e.g. contact 30 on socket E1 should be wired to contact 10, board ED, and contact 40, board E2)

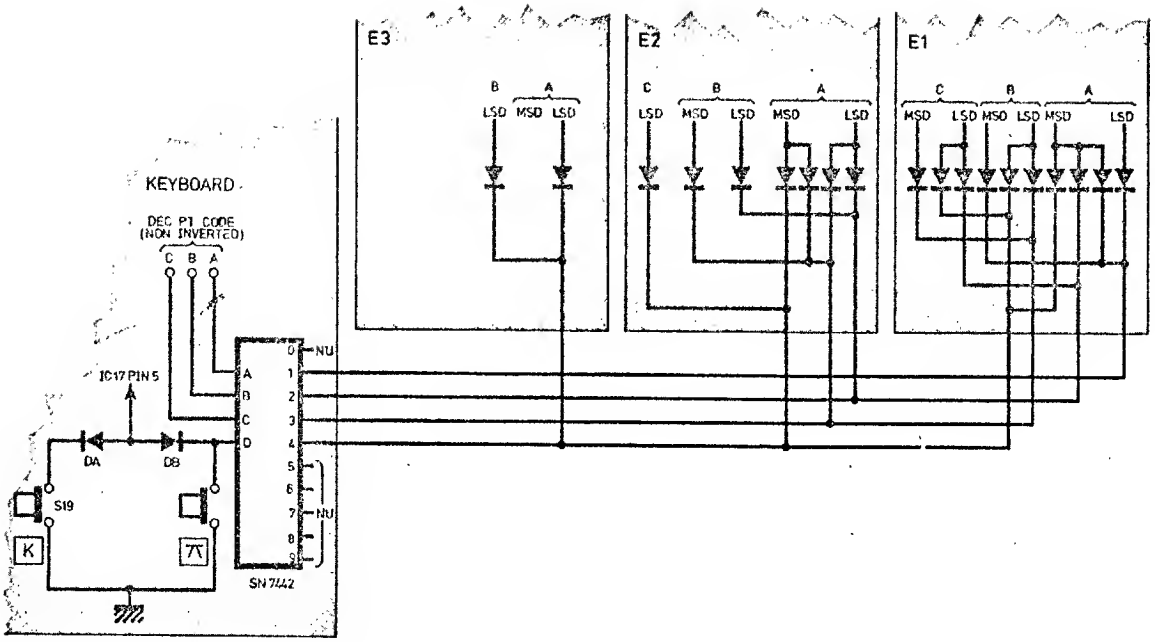


Fig. 5.8. Extra wiring to allow for a fixed constant key in addition to the K key. The diodes shown allow for the number π or a close approximation, to be placed in the entry register when a single key is depressed. The SN7442 is an extra i.c., space for which can be found on the Keyboard panel

INTERCONNECTION AND TESTING

Under chassis edge connector wiring can be started early in the construction sequence to allow operational testing to be carried out as necessary, and this task can be readily completed by referring to the edge connector layout and wiring tables (Fig. 5.7).

The tables are easier to use than wiring diagrams their instructions being implemented by simply wiring the edge connector pin required to all (or any part as required) of the destination listed.

When the register section of one or more of the boards is completed, keyboard entries should be possible by pressing a sequence of number keys, provided of course that the display and keyboard are already functioning, and that the required CLOCK, CLEAR, and data interconnections have been made.

Table 5.1 EXAMPLE OF FIXED CONSTANT KEY DIODE PLACING

Dec. pt setting	Required "π" value	Decimal digit identification: Board E3 M.S.D.	Board E3 L.S.D.	Board E2 M.S.D.	Board E2 L.S.D.	Board E3 M.S.D.	Board E3 L.S.D.	B.C.D. digit
1	3·1					×		D
								C
						×	×	B
								A
2	3·14						×	D
					×			C
					×	×		B
								A
3	3·142					×		D
				×				C
				×			×	B
					×			A
4	3·1416				×		×	D
			×				×	C
			×	×		×		B
								A

The only temporary test connection required to render the circuit operational is a ground connection to the CLEAR buffer gate input to prevent a permanent CLEAR signal being produced.

FIXED CONSTANT OPTION

SN7401 open collector gates are used in the RECALL K path in preference to SN7400 gates because they can be used to perform the "Wired OR" function at their outputs. In practical terms this means that it is possible to "get at" the SN7474 PRESET inputs for use with other data sources than the constant register without altering existing logic.

This possibility opens the door to all sorts of custom modifications to enhance the usefulness of Digi-Cal, and to show how simple some improvements can be, let us consider a scheme for entering a constant which is very commonly used, without taking up space in the constant store itself.

The constant is the ubiquitous Pi (π), but in fact any constant which is likely to be often used is suitable for our purposes, the object being to have the chosen constant always available at the press of its own *separate* key, without interfering with the operation of the constant store which remains available for routine use.

This modification requires only the incorporation of a number of diodes into the ENTRY register boards and the addition of an extra "PI" key on the keyboard with a single extra i.c. The circuit for such a scheme is shown in Fig. 5.8.

An extra diode must be connected to the keyboard logic panel (Fig. 4.2), between the top of the "K" switch S19 and pin 5 on IC17, the previous direct connection being broken. This diode, marked DA in Fig. 5.8, together with diode DB forms an OR gate so that pressing either key "K" or "π" causes the automatic normalisation to be inhibited.

OPERATION OF CONSTANT FACILITY

The principle of operation is that when the "PI" key is pressed one of the outputs of the SN7442 decoder will go low, depending on the setting of the decimal point switch.

The energised output is used to PRESET a number into the ENTRY register via diodes wired in wherever a "1" is required. The diodes are connected to the PRESET inputs at the points marked in Fig. 5.3, and perform the "Wired OR" function with the SN7401 outputs.

The whole circuit acts as a diode "Read Only Memory," where the contents of the memory are programmed at the construction stage by wiring in diodes where required.

The memory contains four separate numbers to allow for the four possible decimal place selections. Table 5.1 shows how the placing of the diodes is determined, a cross marking the position of each.

This circuit can be very useful if Digi-Cal is to be used for calculations containing an often used constant, and can be substituted for the constant store *or* used to complement it. If this option is never likely to be taken up it would be possible to use SN7400 gates in the RECALL path instead of the SN7401s and resistors, but note that the pin connections for the SN7400s are different.

Next month: Logic and construction of A and Z registers.

NEWS BRIEFS

New Data Transmission Technique

A NEW technique of data transmission is to be tested in a forthcoming experiment involving the Post Office and computer manufacturers and users. The system is known as "packet switching" and is basically the transmission of computer data in self-contained, addressed blocks like a series of high speed telegrams.

The user of such a system sends out the data together with the address of its destination and the data is automatically routed to that destination by the system. The need to set up a direct link between sender and receiver before transmission is thus eliminated.

Circuits connecting packet switching exchanges can be used for carrying packets sent by other customers in the time intervals between packets in a series making up a complete message. Because many signals travel on the same wire a large number of low capacity connections to a multi-access computer can be replaced by a single high capacity connection.

The system has the advantage of lower error rates than conventional systems and enables two terminals with different data transmission rates to be connected.

New Range of Calculators

A RANGE of five new electronic calculators has just been announced by the British firm Advance Electronics Ltd.

Because of large scale integration whereby all the electronics can be placed in a handful of discrete packages, assembly costs of complex instruments have been reduced drastically. The features which Advance are promoting are reliability and value for money rather than such dubious advantages as extreme miniaturisation.

The new range consists of four desk-top calculators known as the Executive 16 range and a pocket-sized calculator known as the Executive.

The Executive 16 range all feature 16 digit capability and a keyboard specially designed for high speed work. The keyboard allows a key to be pressed even when another has already been pressed providing that they are released in the correct order.

The basic model (retailing at £95) has the four basic arithmetic operations as well as a "%" key.

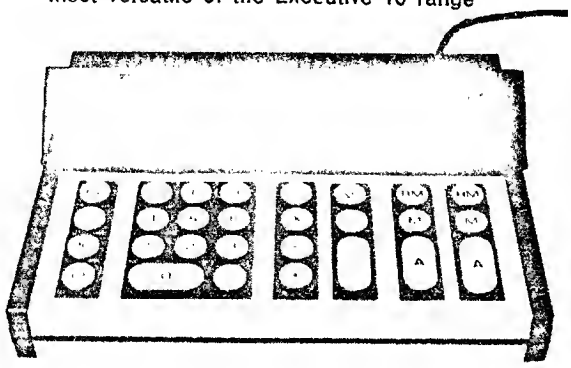
The 16 + 1 (at £115) has a versatile memory with full 16 digit capacity which can also function as an accumulator for automatic list totalling.

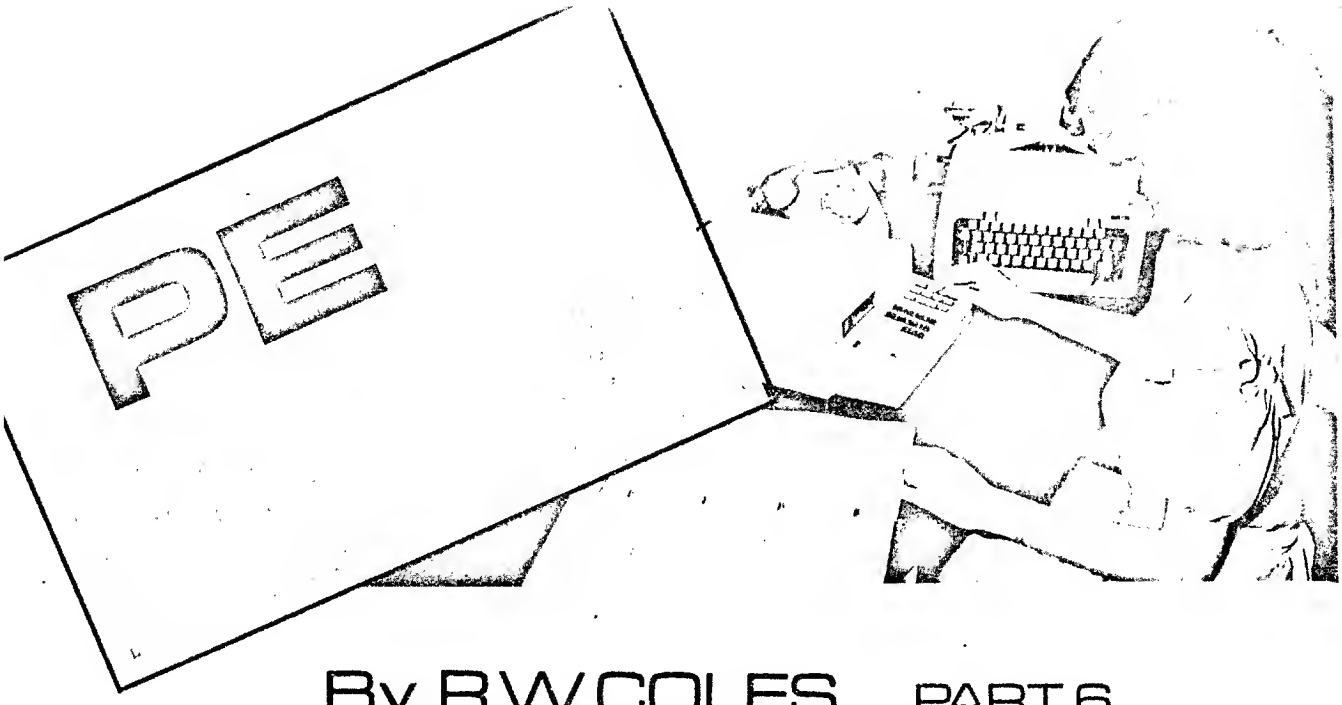
The 16 + 2 (at £145) is specially suitable for V.A.T. calculations featuring two memories.

The 16R (at £175) has all the features of the 16 + 2 but also includes a square root key.

The fifth member of the range is an eight-digit portable (at £52·50) with a plinth for desk use and mains power supply option extras.

Shown here is the Executive 16R which is the most versatile of the Executive 16 range





By R.W.COLES PART 6

ANSWER (A) AND Z REGISTERS

LAST month the construction of the ENTRY register was described together with the constant store and a fixed constant option. To follow this the logic and construction of the two registers which form the main part of the arithmetic section will be described, these being known as the ANSWER (A) register and the Z register.

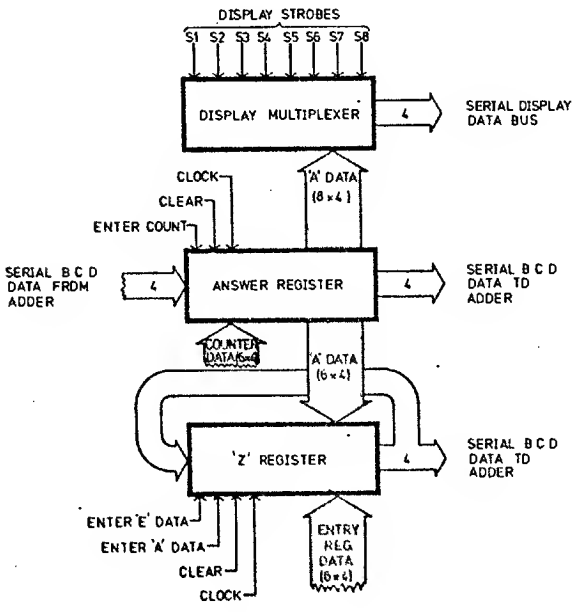


Fig. 6.1. Block diagram of the "A" and "Z" register sections of Digi-Cal

"A" AND "Z" REGISTERS

The A (ANSWER) and Z registers, together with the adder to be described next month, form the heart of the arithmetic unit of Digi-Cal. These registers are identical in capacity, being four (B.C.D.) digits "wide" and ten (decimal) digits "long". They differ in the type of input and output facilities which include both serial and parallel transfers.

Both are right-shift types, and are capable of shifting data at more than one million bits per second in the serial mode, when supplied with suitable clocking signals.

The A register has an associated display multiplexer which is used to send the answer data down the display bus under the control of the display strobes provided by the display board previously described in Part 3.

The multiplexer is identical in principle to the ENTRY register version, but is two (decimal) digits longer to allow display of a full eight digit answer. The most significant two digits are not displayed and are used to allow error detection and decimal point manipulation.

A block diagram of the A and Z register sections of Digi-Cal is given in Fig. 6.1 and this should be studied in conjunction with the overall system block diagram (Fig. 1.3) from the July edition, which did not include the display multiplexer.

REGISTER PARTITIONING

The division of the register circuitry to suit the constraints of a standard printed circuit system requires a good deal of thought to produce an arrangement which:

(a) uses a minimum of "wasted" i.c. positions, and thus the minimum number of separate boards;
(b) shares the number of input/output connections equally between boards so that one board does not demand more edge connector positions than are available on the standard board; and

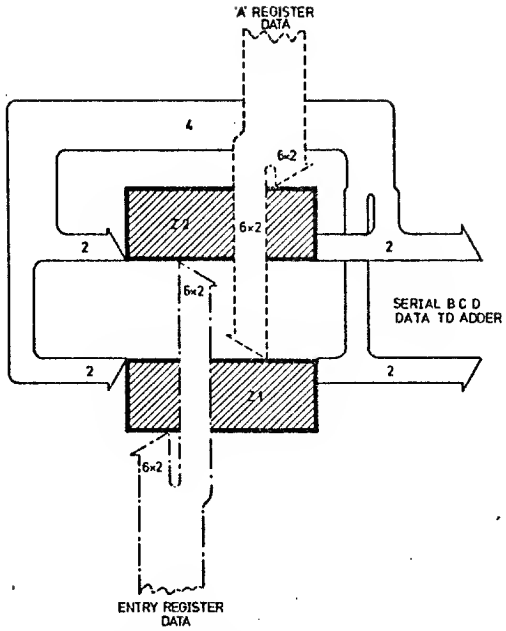


Fig. 6.2. The partitioning of the "Z" register is shown here, together with the inputs and outputs

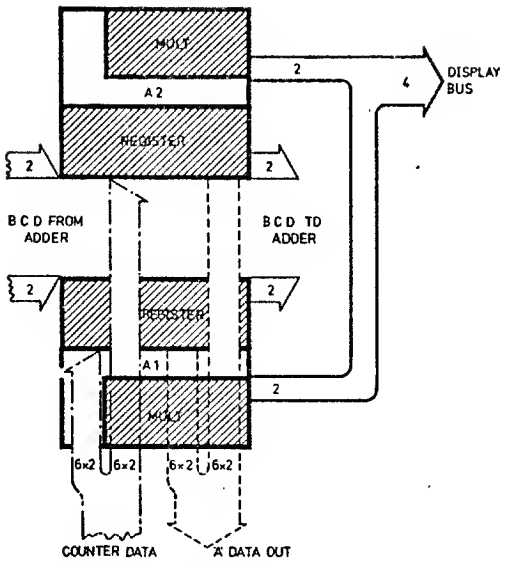


Fig. 6.3. The partitioning of the "A" register into the two halves known as the A1 and A2 registers is shown here

(c) gives a layout arrangement which permits the interchange of identical halves of the circuit and thus cuts down the number of different types of board required.

With the ENTRY register last month, the circuit was divided vertically into three boards each carrying a two digit long register of B.C.D. width, plus a separate multiplexer board.

The A and Z registers on the other hand are divided horizontally into two ten-digit long registers, each two digits wide, giving four boards in all. The A register multiplexer is also split in this way, and in this case is incorporated on the same boards as the register proper.

All this sounds a little complicated but is easier to understand with reference to Fig. 6.2 and Fig. 6.3.

"A" REGISTER

The A register is built on two DL109/44 cards, each of which houses eight TTL i.c.s, two resistors, and two decoupling capacitors.

Making a register ten digits long and four wide would require twenty SN7474 dual D-type flip-flops as used in the ENTRY register, and this number would take up a lot of room, as well as presenting a mammoth wiring-up problem.

Fortunately the TTL series of complex functions known as medium scale integration (M.S.I.) contains a number of ready-made shift register circuits, and it is one of these, the SN7496, which is employed in the A register circuit.

A diagram of the SN7496 is shown in Fig. 6.4, and as can be seen this i.c. consists of a complete five-bit serial shift register in a 16 pin D.I.L. package.

The register comes complete with gating to allow a five-bit parallel input transfer when the PRESET input is activated, and has a separate output from each stage to allow parallel output transfers.

The CLEAR input will set all the flip-flops to the logic "0" output state, and is used to erase the stored contents of the register.

By connecting two of these i.c.s in series a ten-digit register is formed, and by using four of these ten-digit sections, the required A register capacity is achieved, using eight SN7496 i.c.s (see Fig. 5.5).

OPERATION OF "A" REGISTER LOGIC

When an arithmetic programme is running, the data in the A register is shifted serially into the ADDER circuit, in synchronism with the data in the Z register which is either added to or subtracted from the A data.

The output of the ADDER forms the serial input of the A register, so that after a group of ten clock pulses, the A register contains the sum (or difference) of the original A and Z register contents.

If the arithmetic operation required is MULTIPLICATION, then the contents of the A register have to be duplicated in the Z register before the series of additions take place, and to facilitate this the parallel outputs of the A register are used to provide a single 24 bit transfer.

At the end of a DIVISION, the answer is represented by the state of the counter, and before this can be displayed it has to be transferred to the A register. This is also carried out in a single 24 bit transfer, this time using the parallel PRESET inputs of the SN7496s.

In each of these transfers the initiation is provided by a control pulse from the programme.

MULTIPLEXER

The multiplexer consists of a series of SN7401 open-collector gates, with their outputs "wired-OR" to give the required four-bit data-bus. It is formed in the same way as the ENTRY register multiplexer.

The eight strobes or "character call-up" lines are produced in a sequence starting at the most significant end of the register, each one activating a group of four gates to send a single B.C.D. group to the display.

In the case of this multiplexer, the data-bus is produced in two, two-bit halves as a consequence of the partitioning arrangement mentioned earlier. This division of the multiplexer into two physically separate sections means that the display strobes have to be connected to both board A1 and board A2.

"Z" REGISTER

Like the A register, the Z register is housed on two DL109/44 plug-in cards. This register is identical in size to the A register, being ten by four in format, but because of its different role in the arithmetic operations of the calculator, different integrated circuits are employed.

A glance at Fig. 6.1 shows that the Z register is required to accept parallel transfers from two sources, the A register and the ENTRY register. It is not required to provide parallel outputs, only serial outputs being needed to feed the ADDER.

These different input/output requirements preclude the use of SN7496 shift register elements, since these devices can only accept a single parallel input transfer without extensive external gating. Luckily, it is still possible to enjoy the advantages of M.S.I. in this circuit because another device which suits our needs, the SN7494, is available.

The SN7494 is a four-stage serial shift register element with provision for parallel loading from two separate sources, under the control of internal gating.

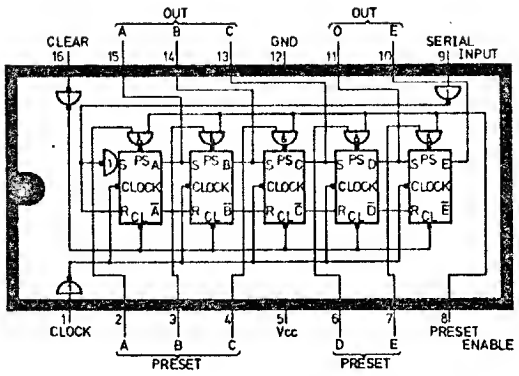


Fig. 6.4. The internal logic of the SN7496 integrated circuit

A logic diagram of this device is shown in Fig. 6.6 where is can be seen that the two sets of parallel inputs, 1A to 1D and 2A to 2D are presented to the PRESET inputs of the flip-flops via four AND-OR-INVERT gates, the appropriate set of input data being selected by the PRESET1 or PRESET2 control line.

Note that output connections are not provided from the A, B, and C flip-flops, which as previously stated, is quite satisfactory for this application.

REGISTER ASSEMBLY

Connecting two SN7494s in series gives a register eight digits long, which falls short of the requirement of ten digits. Therefore two more stages are added

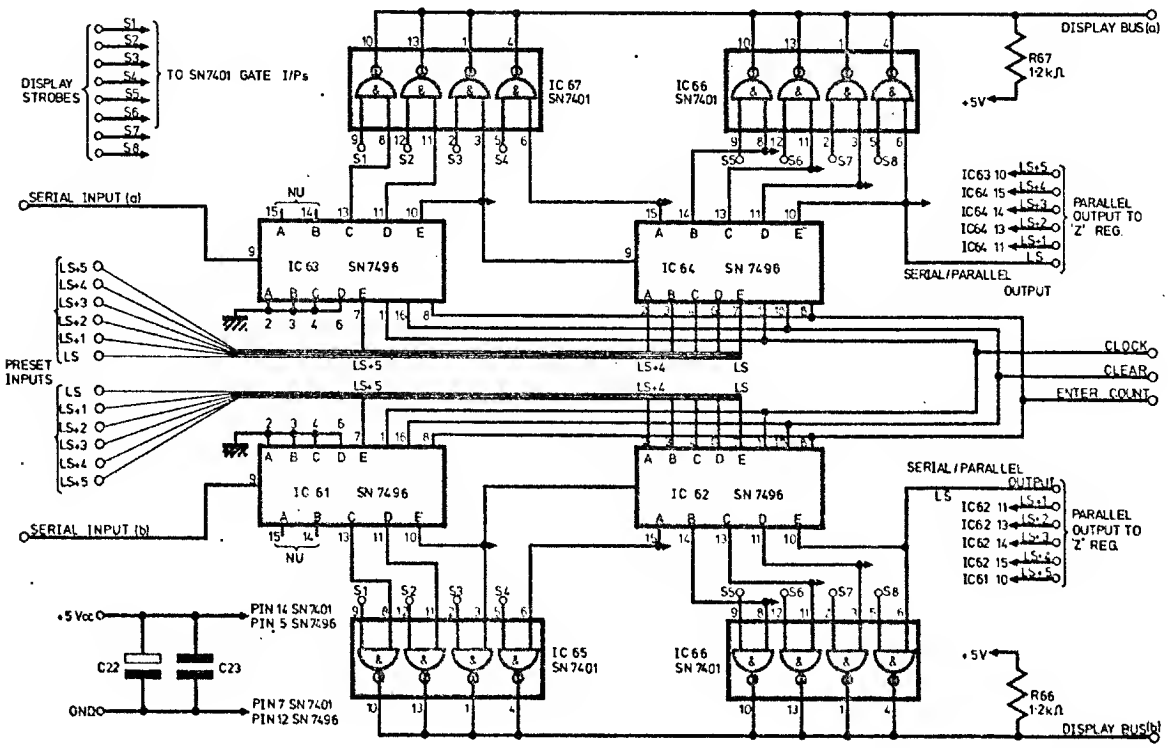


Fig. 6.5. The logic contained on the A1 register board. The A2 board is identical to this

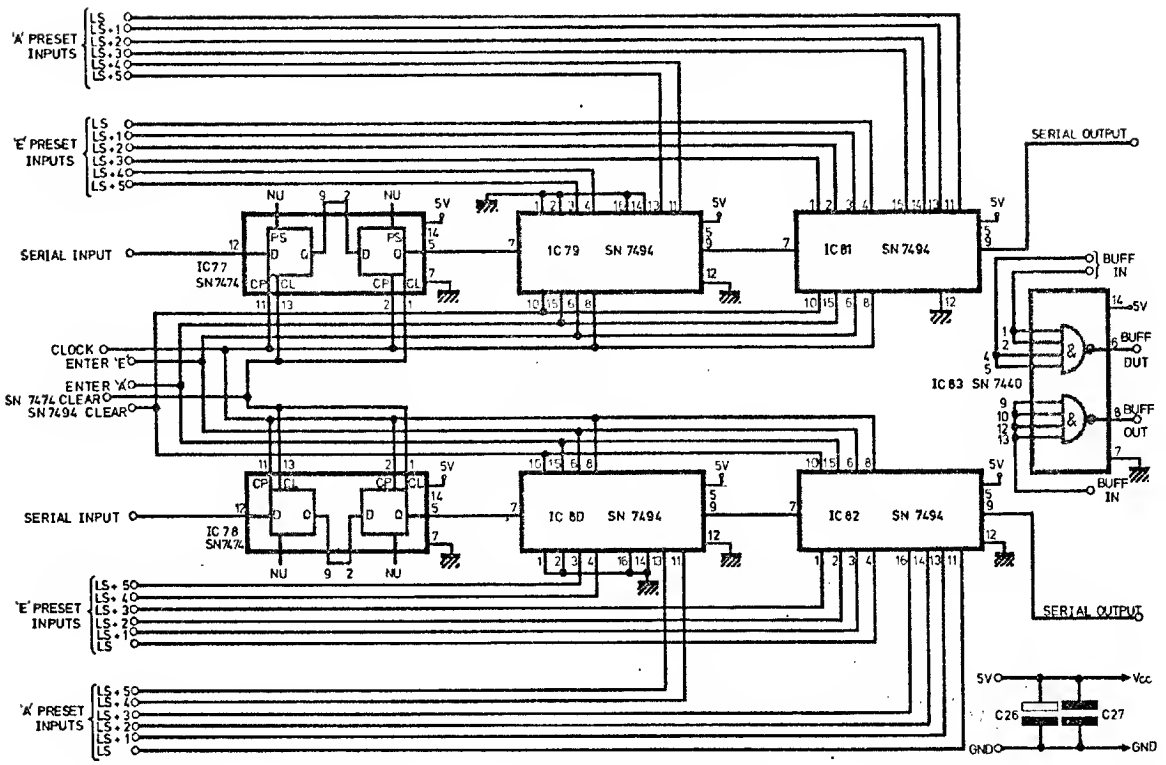


Fig. 6.7. The logic contained on the Z1 register board is shown here. The Z2 board is identical to this

in the form of an SN7474 dual D flip-flop. If these extra stages are placed at the "most-significant" end of the register, no extra input gating will be required since only the six "least-significant" stages are required to accept parallel input transfers. This is the approach adopted for the Z register and the resulting circuit is assembled from eight SN7494s and four SN7474s, giving the required total number of 40 flip-flops.

The circuit of one of the two identical Z register boards is shown in Fig. 6.7 where it can be seen that in addition to the shift register components, an SN7440 dual buffer gate is incorporated.

The connections to these gates are made external to the DL109 cards because these gates are used for different jobs on each of the two cards, and

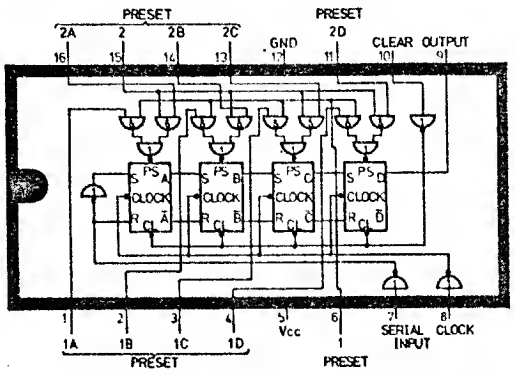


Fig. 6.6. The internal logic of the SN7494 integrated circuit

internal connection would prevent interchanging these when required.

One of the four buffer gates is used to invert the CLEAR Z signal from the programme to make it compatible with the CLEAR inputs of the SN7474 devices, which operate on *low* inputs, as opposed to the SN7494 CLEAR lines which operate on *high* inputs.

The remaining gates are used to buffer the Z register PRESET1 and PRESET2 lines, and in the OVERFLOW logic.

"Z" REGISTER OPERATION

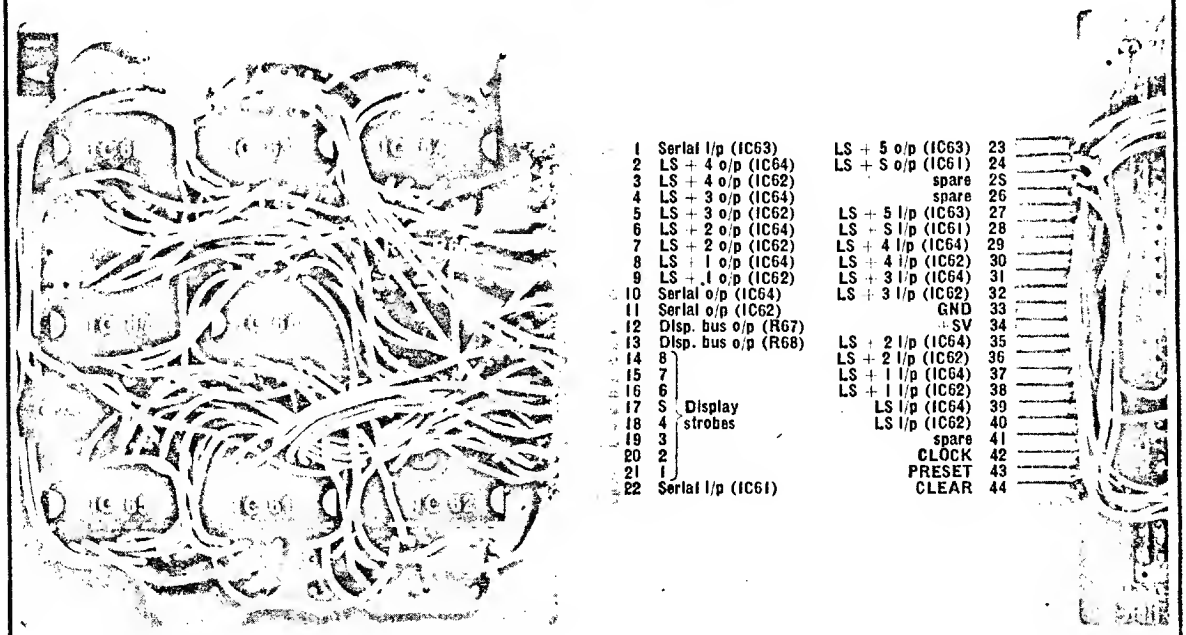
The most important operational aspect of the Z register is that it operates in a recirculating mode, which means that not only is its output fed to the ADDER, but also back to its own input, to give an endless loop.

This feature is important because it means that the register contents are not altered no matter how many bursts of ten clock-pulses are applied in the course of an arithmetic operation.

This facility is required in the MULTIPLY and DIVIDE programmes, where the contents of the Z register are continuously added to or subtracted from the contents of the A register until the result is produced.

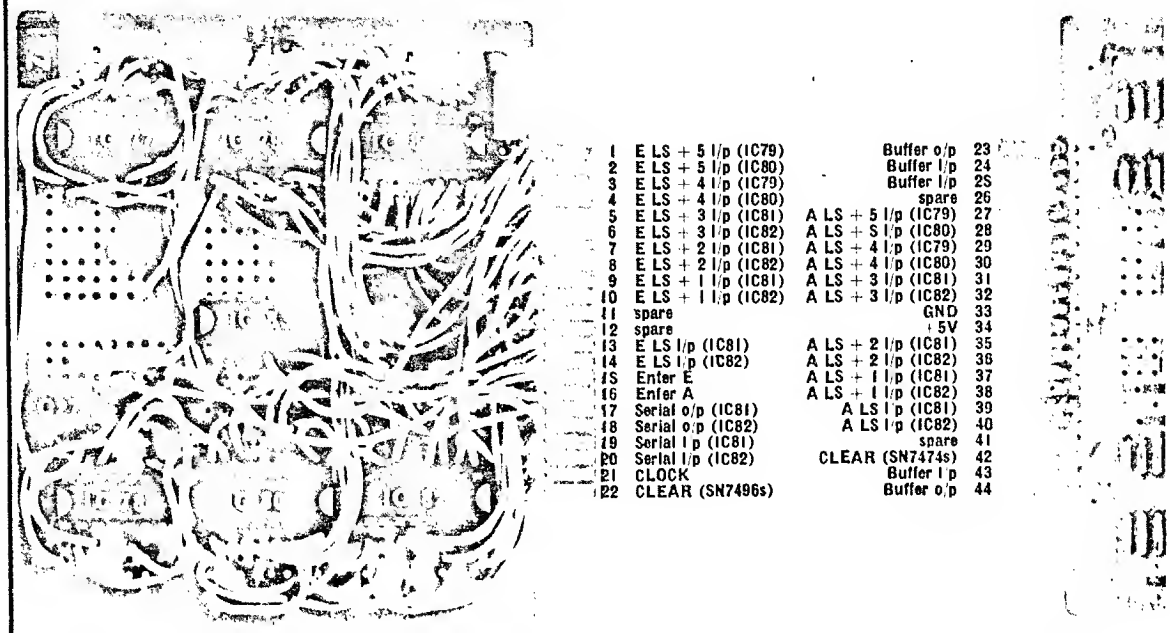
In these programmes the contents of the register can be used up to one million times in a single computation. Of course, this is not to say that the register contents are completely invariant, for when a particular set of data is finished with the register will be cleared by a CLEAR pulse from the programme, ready for new data to be entered in parallel from the ENTRY or A registers.

A AND Z BOARDS



1	Serial I/p (IC63)	LS + 5 o/p (IC63)	23
2	LS + 4 o/p (IC64)	LS + S o/p (IC61)	24
3	LS + 4 o/p (IC62)	spare	25
4	LS + 3 o/p (IC64)	spare	26
5	LS + 3 o/p (IC62)	LS + 5 I/p (IC63)	27
6	LS + 2 o/p (IC64)	LS + S I/p (IC61)	28
7	LS + 2 o/p (IC62)	LS + 4 I/p (IC64)	29
8	LS + 1 o/p (IC64)	LS + 4 I/p (IC62)	30
9	LS + 1 o/p (IC62)	LS + 3 I/p (IC64)	31
10	Serial o/p (IC64)	LS + 3 I/p (IC62)	32
11	Serial o/p (IC62)	GND	33
12	Disp. bus o/p (R67)	+5V	34
13	Disp. bus o/p (R68)	LS + 2 I/p (IC64)	35
14	8	LS + 2 I/p (IC62)	36
15	7	LS + 1 I/p (IC64)	37
16	6	LS + 1 I/p (IC62)	38
17	5 Display	LS I/p (IC64)	39
18	4 strobes	LS I/p (IC62)	40
19	3	spare	41
20	2	CLOCK	42
21	1	PRESET	43
22	Serial I/p (IC61)	CLEAR	44

Fig. 6.8a. Layout of the i.c.s on the "A" register boards and function of the edge contacts, both boards being identical



1	E LS + 5 I/p (IC79)	Buffer o/p	23
2	E LS + 5 I/p (IC80)	Buffer I/p	24
3	E LS + 4 I/p (IC79)	Buffer I/p	25
4	E LS + 4 I/p (IC80)	spare	26
5	E LS + 3 I/p (IC81)	A LS + 5 I/p (IC79)	27
6	E LS + 3 I/p (IC82)	A LS + 5 I/p (IC80)	28
7	E LS + 2 I/p (IC81)	A LS + 4 I/p (IC79)	29
8	E LS + 2 I/p (IC82)	A LS + 4 I/p (IC80)	30
9	E LS + 1 I/p (IC81)	A LS + 3 I/p (IC81)	31
10	E LS + 1 I/p (IC82)	A LS + 3 I/p (IC82)	32
11	spare	GND	33
12	spare	+5V	34
13	E LS I/p (IC81)	A LS + 2 I/p (IC81)	35
14	E LS I/p (IC82)	A LS + 2 I/p (IC82)	36
15	Enter E	A LS + 1 I/p (IC81)	37
16	Enter A	A LS + 1 I/p (IC82)	38
17	Serial o/p (IC81)	A LS I/p (IC81)	39
18	Serial o/p (IC82)	A LS I/p (IC82)	40
19	Serial I/p (IC81)	spare	41
20	Serial I/p (IC82)	CLEAR (SN7474s)	42
21	CLOCK	Buffer I/p	43
22	CLEAR (SN7496s)	Buffer o/p	44

Fig. 6.8b. Layout of the i.c.s on the "Z" register boards and function of the edge contacts, both boards being identical

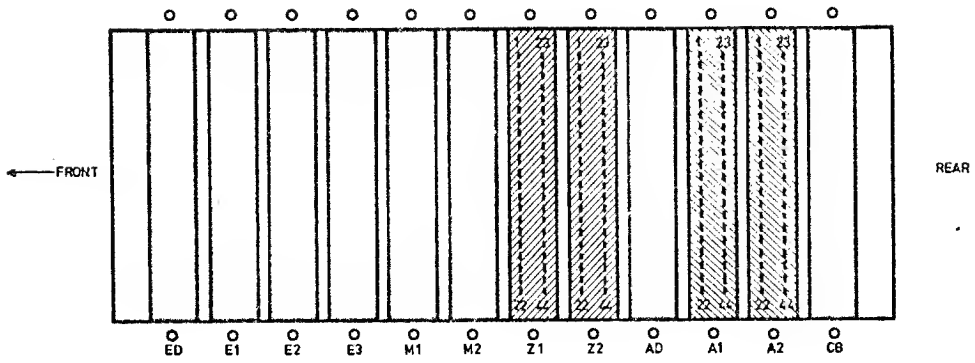


Fig. 6.9. Disposition of the edge connectors as seen from underneath the main chassis plate

CONSTRUCTION

The component layout arrangement for the A and Z register boards is shown in Fig. 6.8.

These boards have a good deal of wiring to the edge contacts due to the large number of parallel input/output wires required, and some care is required in laying this out so as not to produce very long wiring runs or large wiring concentrations.

The registers are required to perform serial shifts at high speed which means that the interconnections associated with this aspect of the circuit, i.e. everything except the parallel input/output wiring, should be kept as short as possible to reduce stray capacitance effects. With this in mind it is advisable to wire up the serial interconnections and clock lines before the rest of the wiring (which is not critical) is added.

Wiring is normally carried out on the component side of the DL109/44 boards, but it was found with the prototype that wiring congestion can be alleviated on the A1 and A2 boards by connecting the parallel output wiring to the edge contacts on the underside of the board.

EDGE CONNECTOR INTERCONNECTIONS

The edge connectors for these registers occupy the Z1, Z2, A1, and A2 positions on the chassis assembly (see Fig. 6.9), and are wired up in accordance with the wiring tables given. These tables (Fig. 6.10) are used by simply connecting the pin number required to the destination or destinations listed next to it in the table.

Each of these tables is complete, which means that a wire from the A register to the Z register will be listed in both the A *and* the Z register tables, so be sure to keep a record of wiring already carried out to prevent unnecessary duplication.

Again it is advisable to keep the wiring associated with serial transfers as direct as possible, and it is an idea to use a different coloured wire for these interconnections so that they may be easily identified later.

Where these serial data and clock lines exceed a few inches in length they should be routed as close to the chassis metal as possible to take advantage of its "ground-plane" properties. Interconnections to be treated with care are marked with an asterisk in Fig. 6.10.

Z1

E3/9	1	23	Z1/15, Z2/15
E3/10	2	24	enter E (prog)
E3/15	3	25	from E* logic
E3/16	4	26	not used
E2/9	5	27	A1/23
E2/10	6	28	A1/24
E2/15	7	29	A1/2
E2/16	8	30	A1/3
E1/9	9	31	A1/4
E1/10	10	32	A1/5
not used	11	33	GND
	12	34	+5V
E1/15	13	35	A1/8
E1/16	14	36	A1/7
Z1/23	15	37	A1/8
Z2/23	16	38	A1/9
*Z1/19	17	39	A1/10
*Z1/20	18	40	A1/11
*AD/19, Z1/17	19	41	not used
*AD/20, Z1/18	20	42	Z1/44
*CB/1	21	43	CB/13
CB/13	22	44	Z1/42, Z2/42

Z2

E3/7	1	23	Z1/16, Z2/16
E3/8	2	24	enter A (prog)
E3/13	3	25	not
E3/14	4	26	used
E2/7	5	27	A2/23
E2/8	8	28	A2/24
E2/13	7	29	A2/2
E2/14	8	30	A2/3
E1/7	9	31	A2/4
E1/8	10	32	A2/5
not used	11	33	GND
	12	34	+5V
E1/13	13	35	A2/6
E1/14	14	36	A2/7
Z1/23	15	37	A2/8
Z2/23	16	38	A2/9
*Z1/19	17	39	A2/10
*Z2/20	18	40	A2/11
*AD/17, Z2/17	19	41	not used
*AD/18, Z2/18	20	42	Z1/44
*CB/1	21	43	not
CB/13	22	44	used

A1

*AD/5	1	23	Z1/27
Z1/29	2	24	Z1/28
Z1/30	3	25	not
Z1/31	4	26	used
Z1/32	5	27	M2/25
Z1/35	6	28	M2/26
Z1/36	7	29	M2/29
Z1/37	8	30	M2/30
Z1/38	9	31	M2/35
*AD/9, Z1/39	10	32	M2/36
*AD/10, Z1/40	11	33	GND
To display data bus I/p B	12	34	+5V
To display data bus I/p A	13	35	M1/25
	14	36	M1/28
Io	15	37	M1/29
display	16	38	M1/30
board	17	39	M1/35
strobe	18	40	M1/36
outputs	19	41	not used
	20	42	CB.18*
	21	43	CB/16
*AD/6	22	44	CLEAR (prog)

A2

*AD/3	1	23	Z2/27
Z2/29	2	24	Z2/28
Z2/30	3	25	not
Z2/31	4	26	used
Z2/32	5	27	M2/25
Z2/35	6	28	M2/26
Z2/36	7	29	M2/29
Z2/37	8	30	M2/30
Z2/38	9	31	M2/35
*AD/7, Z2/39	10	32	M2 36
*AD/8, Z2/40	11	33	GND
To display data bus I/p D	12	34	+5V
To display data bus I/p C	13	35	M1/23
A1/14	14	36	M1/24
A1/15	15	37	M1/27
A1/18	16	38	M1/28
A1/17	17	39	M1/31
A1/16	18	40	M1/32
A1/19	19	41	not used
A1/20	20	42	CB/18*
A1/21	21	43	CB/16
*AD/4	22	44	CLEAR (prog)

Fig. 6.10. Interwiring details of the four edge connectors holding the "A" and "Z" register boards. The asterisks show connections which need special care.

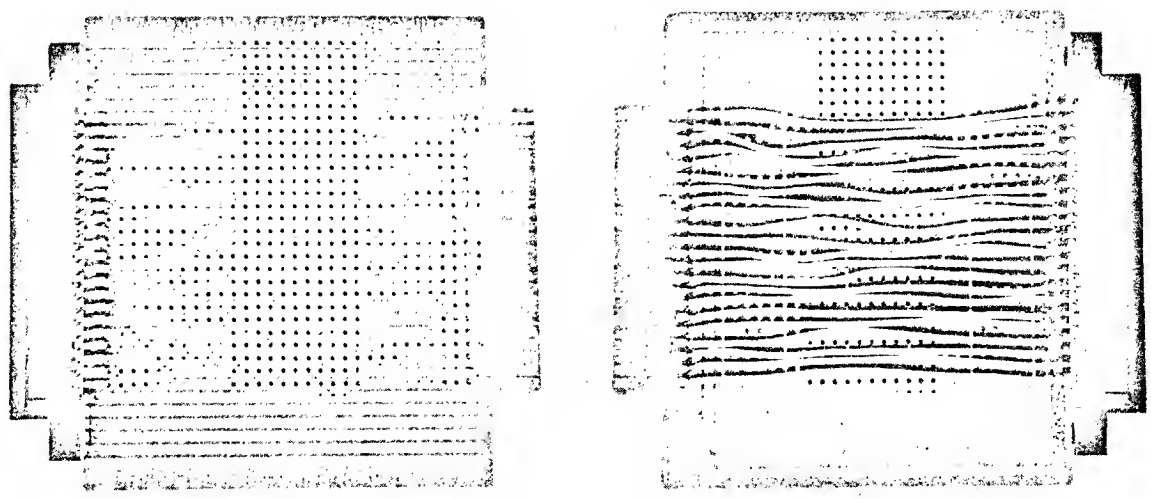


Fig. 6.11. Construction of a 44-way extension board which makes possible testing of boards in situ

TESTING

Testing these boards in an operational way is difficult at this stage and until the CLOCK board is constructed there is little that can be done except a check that the power supply lines are connected properly. For this reason it is essential that all wiring is double checked to remove wiring-up errors before proceeding.

EXTENSION BOARD

When the calculator nears completion and tests are possible in an operational situation, it will some times be required to measure a logic level, or inspect an interconnection while the logic boards are still connected in the circuit. As things stand this would prove difficult because of the close packing of the DL109 cards in their respective edge connectors.

To overcome this problem it is possible to construct an extension board which, when interposed between a particular board and its edge connector, has the effect of raising the board into a position where all its components and associated wiring are readily accessible, while still electrically connected to the rest of the circuit.

The layout for such an extension is shown in Fig. 6.11 where it can be seen that the component parts are simply an edge connector and a Shirehall DL107 board, together with some wiring.

The DL107 card is of the same physical size as a DL109, but instead of a printed wiring pattern to accept nine D.I.L. i.c.s, the DL107 has a Veroboard type of matrix, orginally intended for wiring up discrete components.

The construction of the extension consists of simply soldering the 22 ways of one half of the edge connector to the DL107 strips which terminate in gold plated edge contacts, then using single core wire to connect the other 22 edge connector tags to the corresponding DL107 edge contacts on the reverse side of the board.

COMPONENTS

A1, A2 BOARDS

Resistors
R67–R70 1·2kΩ ¼W ±10% carbon

Capacitors
C22, C24 10μF 15V elect. (2 off)
C23, C25 0·047μF (2 off)

Integrated Circuits
IC61–64, IC69–72 SN7496 (8 off)
IC65–68, IC73–76 SN7401 (8 off)

Printed Circuit boards and sockets
Type DL109/44 boards (Shirehall) (2 off)
Type DPK165 edge connectors (Shirehall) (2 off)

Z1, Z2 BOARDS

Capacitors
C26, C28 10μF 15V elect. (2 off)
C27, C29 0·047μF (2 off)

Integrated Circuits
IC77, 78, 84, 85 SN7474 (4 off)
IC79–82, IC86–89 SN7494 (8 off)
IC83, IC90 SN7440 (2 off)

Printed Circuit Boards and Sockets
Type DL109/44 boards (Shirehall) (2 off)
Type DPK165 edge connectors (Shirehall) (2 off)

(In each case components are divided equally among the two boards which make up the A and Z registers)

The physical strength of the assembly can be improved by using a fillet of Araldite to join the edge connector and the DL107.

This simple servicing aid can come in very handy when testing any of the twelve Digi-Cal logic boards.

Next month: Clock Board.

THE subject of this month's article is the clock generator board which has the function of generating a range of timing pulses for use throughout the arithmetic operations. A single capacitor is used to control the speed at which the whole system operates and this fact means that by running the system at slow speed, faults become relatively easy to trace.

CLOCK BOARD

The circuit and logic of the clock pulse generating board is more interesting than, say, the shift register boards because of the diversity of the logic operations performed. The tasks which this circuit is called upon to carry out are listed below:

(a) Generate batches of ten clock pulses for the A, Z, and AD boards when instructed to do so by the programme. During addition or subtraction a single batch is required whereas during multiplication or division batches are produced continuously until detection logic decides that the arithmetic operation has been completed.

(b) Generate a single batch of n (or 10-n) clock pulses when instructed to do so at the beginning of the MULTIPLICATION programme and the end of the DIVISION programme respectively to clock the A, Z, and AD boards. These clock pulses are used for decimal point positioning purposes, where n is less than ten and is determined by the setting of the decimal point thumbwheel.

(c) Provide an ungated clock pulse output to operate the programme counter and the ENTRY register normalisation system.

(d) Generate a single output pulse for every batch of ten clock pulses produced so that the number of batches can be counted during the MULTIPLICATION and DIVISION programmes. This pulse to be generated *during* the batch generation time, to offset propagation delay problems.

(e) Generate a single output pulse at the *end* of each batch of clock pulses for use with the OVERFLOW detection logic.

(f) Generate an output to restart the programme sequence at the end of the series of additions or subtractions carried out during multiplication and division.

(g) Provide an isolated buffering circuit for the large load represented by the A board PRESET input. (This buffer is not connected with any of the other clock circuits.)

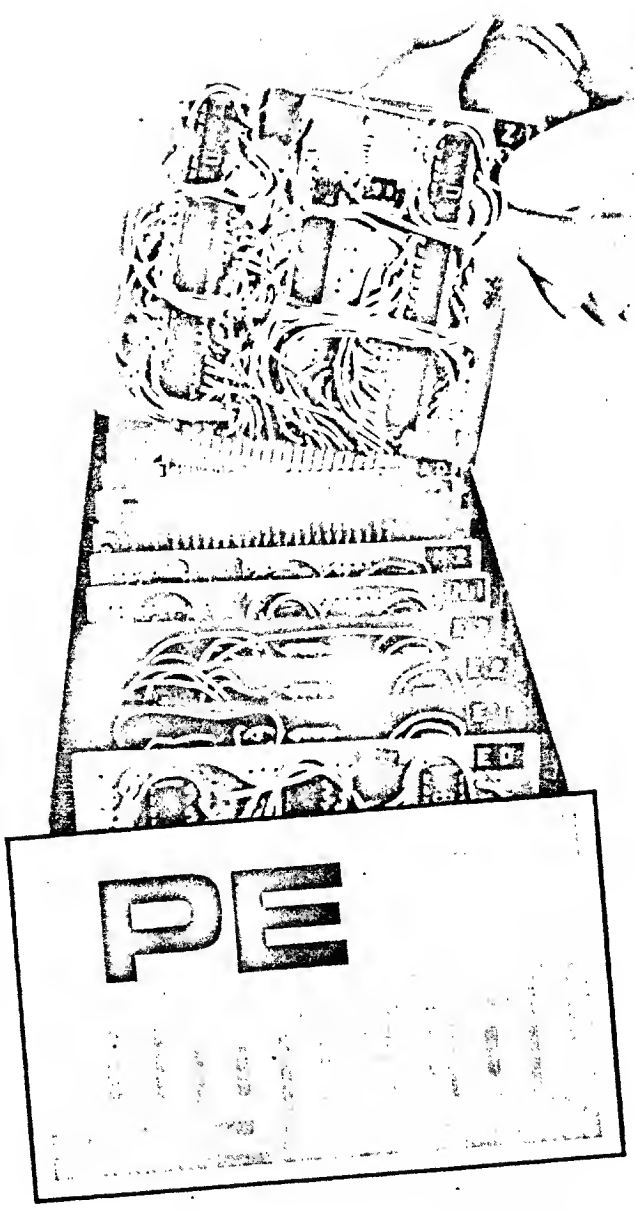
BASIC CIRCUIT

The heart of the CLOCK board is the circuit which produces a batch of ten pulses on demand, all other requirements being met by modification of this basic logic arrangement, which is shown in Fig. 7.1.

The "clock" shown in Fig. 7.1 is simply a square wave oscillator, and this is used to trigger a four-stage, decade counter via a single gate.

The counter will register each of the clock pulses until the tenth one sets the decade counter back to the 0000 state.

This event is detected by the output of the D counter stage falling, and is used to clock a D type flip-flop which has its data input (D) connected to a level "1" gate output (STOP CLOCK signal). When



By R.W.COLES

PART 7

CLOCK GENERATOR BOARD

the counter clocks the flip-flop in this way the STOP CLOCK input causes the flip-flop Q output to go to a "1" level and its $\overline{Q}$ output to go to a "0" level.

The "0" level output from the $\overline{Q}$ side of the flip-flop is connected back to the gate in series with the clock input to the counter, and has the effect of preventing any further pulses from getting through to the trigger input.

If at some future time another batch of ten pulses is required, the flip-flop can be reset via its CLEAR input, whereupon the sequence is repeated.

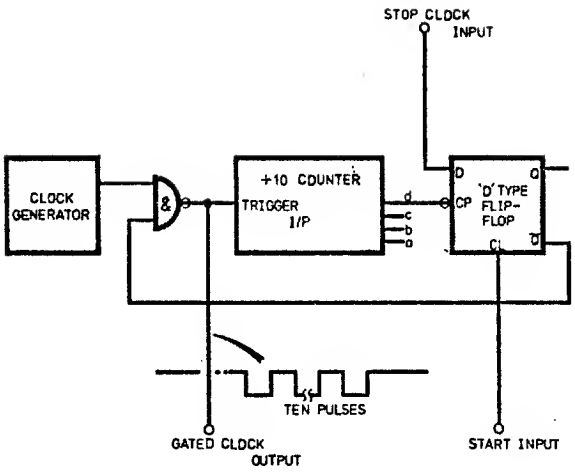


Fig. 7.1. This diagram shows the heart of the clock generator board

If more than one batch of ten pulses is required the STOP CLOCK input can be left in the "0" state so that when the flip-flop is clocked at the end of ten pulses, its $\overline{Q}$ output remains in the "1" state.

When sufficient batches have been produced the STOP CLOCK input can be taken to the "1" condition so that at the end of the next batch the clock is shut off.

Note that with this system no matter how long the clock is allowed to run before being stopped the total number of clock pulses produced will always be divisible by ten, and this is obviously essential for the correct operation of Digi-Cal.

If a smaller number of clock pulses were produced during any batch, the answer produced would be in error by one or more powers of ten.

FULL CIRCUIT

The full clock circuit is shown in Fig. 7.2 and as can be seen a considerable amount of extra gating has been added to modify the basic circuit to enable it to perform all the tasks listed earlier. To make

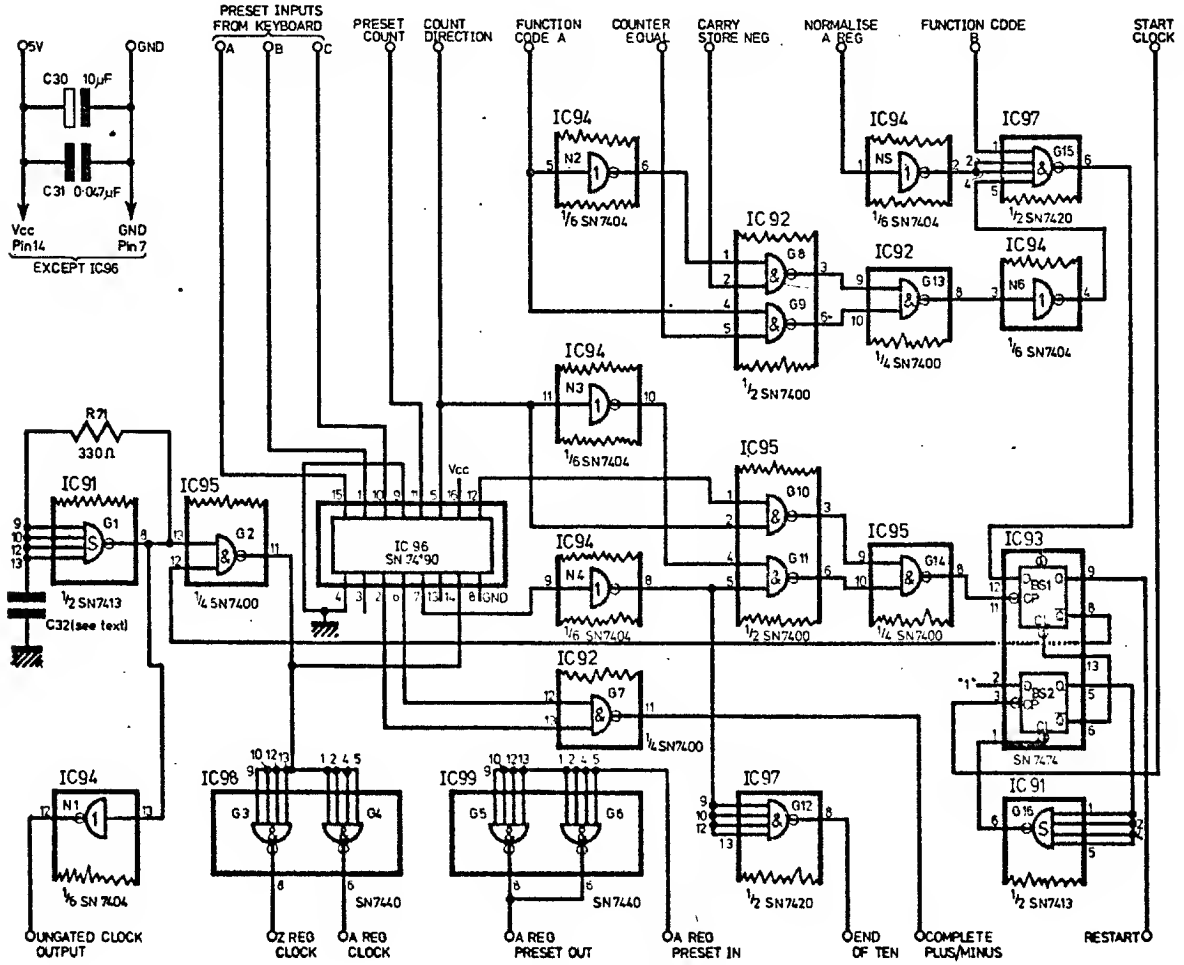


Fig. 7.2. The full circuit diagram of the clock generator board

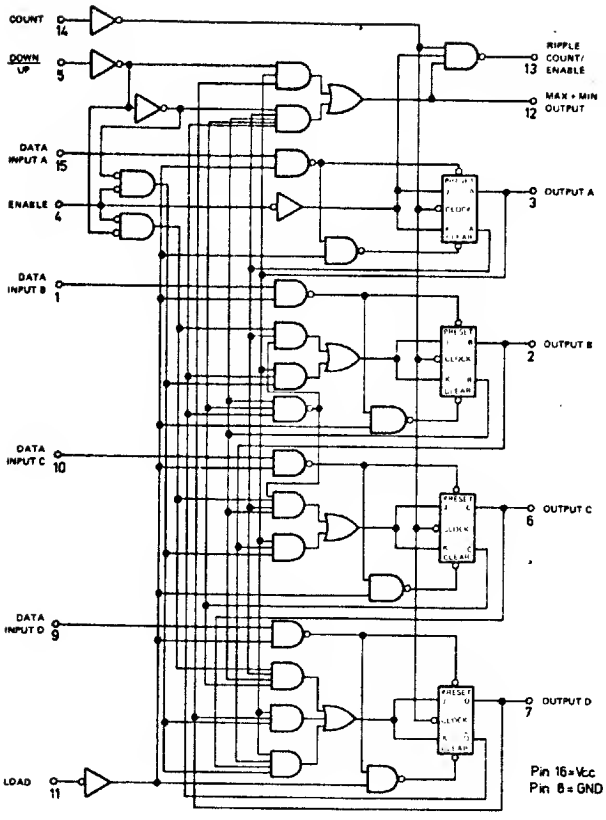


Fig. 7.3. The internal logic of the SN74190 reversible counter with pin numbers of the D.I.L. package

the circuit easier to follow, the gates have not been rigidly constrained within a square box as they have been in previous circuits. That kind of approach can make the whole thing look more complicated than it really is where a lot of gating logic is employed.

UP/DOWN COUNTER

The decade counter used on this board is not the ubiquitous SN7490 as may be expected, because although this type of counter would perform satisfactorily in the basic circuit already discussed, it could not be modified to allow it to carry out task (b).

The counter chosen is in fact the SN74190 which incorporates several extra facilities including the ability to count down as well as up, and the provision of parallel data inputs which allow the starting count to be preset to any b.c.d. number from zero to nine.

The logic diagram of this counter is shown in Fig. 7.3 and a glance at this will serve to confirm that being able to buy one of these in a 16 pin package saves a lot of time and money over having to construct such a circuit from separate gates and flip-flops!

Note that apart from the usual clock input and data outputs, there are parallel data inputs and a wide variety of control inputs and outputs whose functions are listed as follows.

DOWN/UP	Decides count direction (i.e. 0 to 0 or 9 to 0)
ENABLE	Allows counting to take place (not required in Digi-Cal)
LOAD	Presets the counter to the condition on the DATA INPUTS
MAX/MIN	Goes to a logic "1" if the counter contains 9 and is counting UP, or 0 and is counting DOWN
RIPPLE COUNT ENABLE	Output used for cascading SN74190 (not required in Digi-Cal)

CLOCK OSCILLATOR

The clock oscillator is very simple and takes advantage of the useful properties of the SN7413 dual, four input, Schmitt trigger gate. The gates in this package have regenerative feedback applied so that they can be operated from slowly changing d.c. inputs without any spurious oscillations being produced as can sometimes occur with the standard TTL gate circuit.

The hysteresis embodied in the input characteristic of the SN7413 makes it ideal for use as a free-running multivibrator for use between 1Hz and 30MHz.

The only components required to form such a multivibrator, in addition to one of the gates in an SN7413 package, are a 330 ohm resistor and a capacitor of suitable value to set the frequency to the required range.

When Digi-Cal is completed the clock frequency will be left set to one value, but during the testing phase it is handy to be able to alter the frequency to a much lower value so that things happen more slowly.

To assist constructors in the choice of capacitor for low frequency operation, Fig. 7.4 shows a graph for reading frequency against capacitor value.

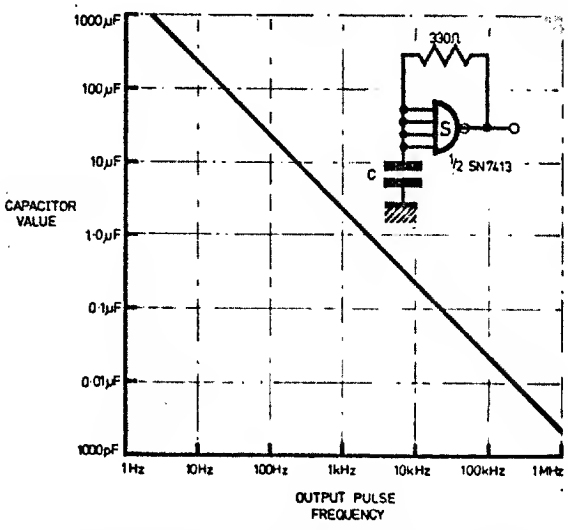


Fig. 7.4. This graph shows the relationship between the clock frequency and the value of the timing capacitor

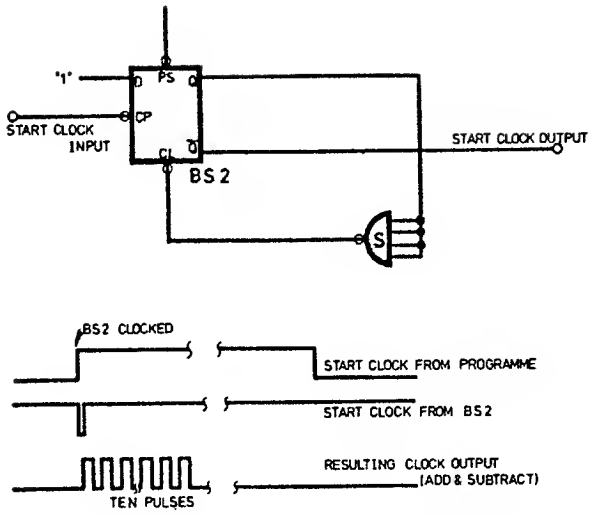


Fig. 7.5. Detail of Fig. 7.2 showing the flip-flop and Schmitt gate used to generate a narrow pulse

COUNTER OPERATION

Using the output of the counter to clock the D-type latch flip-flop is complicated in the full circuit by the need to use different clock stimuli depending on the count direction. This is taken care of by gates G10, G11, G14 and inverters N3, N4 which, depending on the state of the UP/DOWN control line select either the D output or the MAX/MIN output of the counter to feed the SN7474 clock input.

The operation of the counter when generating batches of ten clock pulses is the same as that of the basic circuit, but some extra logic is necessary to start the sequence.

The START CLOCK command arrives as a long pulse from the programme circuits, and because of its length it cannot be used directly to clear BS1. If it was used for this purpose it would start the clock generation satisfactorily, but the ten clock pulses are generated so quickly that when the time came to stop the clock the START CLOCK would still be present and another batch would begin.

To overcome this problem the necessarily long START CLOCK pulse is used to trigger a monostable circuit in the shape of BS2 and G16, which gives a very narrow output pulse which is ideal for clearing BS1.

The use of a flip-flop and a gate as a monostable seems a little strange and to make the operation of this arrangement a little clearer it has been redrawn as Fig. 7.5. The circuit relies upon the normally troublesome "propagation delays" associated with all gates and flip-flops, to allow its operation.

When the rising edge of the START CLOCK pulse arrives it triggers the flip-flop and causes the open circuit or "1" condition to be clocked through from the D input to the Q output. The rising Q output is then used to operate the flip-flop CLEAR input via the SN7413 gate which acts as an inverter *and* a delay element.

When the flip-flop is cleared the circuit returns to its starting condition, ready to be retriggered in the future. The output pulse width (which could be taken from either the Q or the $\overline{Q}$ output) is dependent on the delay in the gate and the delay between a CLEAR input and a corresponding output (this varies from device to device), but gives a pulse of about 30 to 40 ns in practice.

STOP CLOCK INPUTS

The logic decision whether or not to allow the STOP CLOCK input to BS1 to go to a "1" level is a function of five board inputs, and depends on the arithmetic operation in progress.

The logic producing the STOP CLOCK signal comprises gates G8, G9, G13, G15, and inverters N2, N5, N6. The FUNCTION CODE B input (which is a "0" level during ADDITION and SUBTRACTION) and the NORMALISE A REGISTER input (which is a "0" level during the MULTIPLICATION and DIVISION decimal point positioning period) have a direct effect and stop the clock at the end of one batch of pulses.

The COUNTER EQUAL input (which is the basic STOP signal during MULTIPLICATION) and the CARRY STORE NEGATIVE input (which is the basic STOP signal during DIVISION) are allowed to stop the clock when sufficient batches of ten pulses have been produced, and are selected according to the programme used, by the FUNCTION CODE A input. This input is a '0" level for MULTIPLY and a "1" level for DIVIDE.

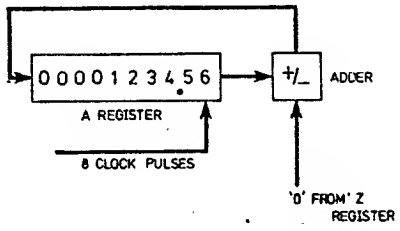


Fig. 7.6. This diagram shows the basic A register and adder sections to illustrate how virtual left shifts are managed

NORMALISATION

The arithmetic section of Digi-Cal does not take account of decimal fractions directly, and treats all numbers as integers. Thus, 2·5 times 2·0 is treated as 25 times 20, giving an answer of 500 which, when displayed, appears as 50·0, instead of 5·0 as required.

The answer reached in this way obviously needs correction, and this is achieved by shifting it to the right by the number of decimal places selected on the thumbwheel. This part of the programme sequence is called NORMALISATION, and is achieved in a different way during DIVISION.

Division of 2·5 by 0·5 leads to an initial answer of 0·5, which suggests a left shift of one place is required, but in practice it is necessary to left shift not the ANSWER, but the DIVIDEND, before the arithmetic process starts. In this way, 2·5 divided by 0·5 becomes 25·0 divided by 0·5, which gives the correct answer of 5·0 without correction.

Left and right shifts such as those described above obviously require a batch of less than ten clock pulses, and this is where the PRESET inputs of the SN74190 are used to advantage. Before looking at

CLOCK GENERATOR BOARD

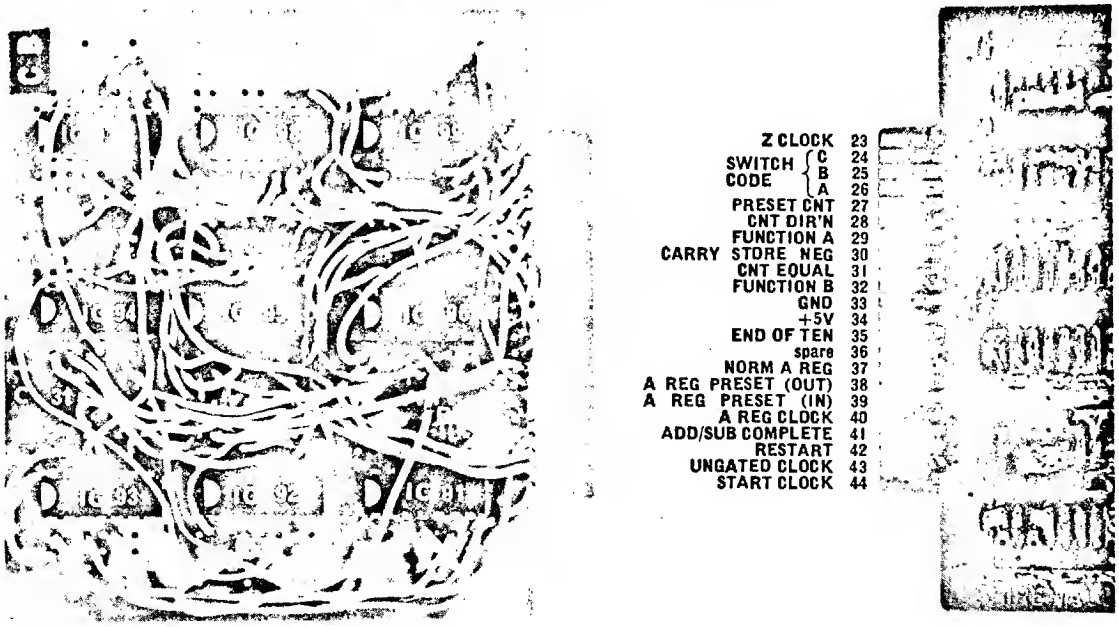
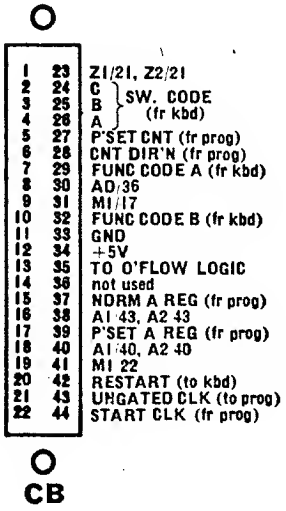


Fig. 7.7. Layout of the components on the clock generator board and function of the edge contacts. Also shown is the wiring details of the edge connector (below left)



COMPONENTS . . .

CLOCK GENERATOR BOARD

Resistors

R71 330Ω ¼W ±10% carbon

Capacitors

C30 10μF 15V elect.
C31 0·047μF
C32 see text

Integrated Circuits

IC91	SN7413
IC92	SN7400
IC93	SN7474
IC94	SN7404
IC95	SN7400
IC96	SN74190
IC97	SN7420
IC98, IC99	SN7440 (2 off)

Printed Circuit Board

Type DL109/22 (Shirehall)

the generation of these shortened batches, it is necessary to look at just how the normally right-shifting A register is made to shift left.

VIRTUAL LEFT SHIFTS

The way in which left shifts are achieved is best studied with the aid of Fig. 7.6 which shows the basic Digi-Cal A REGISTER and ADDER.

The requirement is to shift the number 1234·56 two places to the left, because DIVISION is in progress and the thumbwheel is set to two.

To turn the A REGISTER into a bi-directional type at the hardware level would require considerable numbers of extra gates, not to mention the preclusion of the use of SN7496 devices, and for this reason any such move is undesirable.

Fortunately by employing what amounts to a programming "dodge" it is possible to turn a hardware right shift into a virtual left shift, and this is achieved by clocking the register with 10 minus *n* pulses.

By applying only eight pulses to the register in Fig. 7.6, and by leaving the output of the ADDER unmodified by the Z REGISTER input, the A data recirculates until it ends up as 123456·00.

This system relies on the fact that there are at least *n* zeros to the left of the number to be shifted, and provides one reason why the A and Z registers are ten digits long.

GENERATING LESS THAN TEN CLOCK PULSES

To generate the *n* pulses needed during the MULTIPLICATION NORMALISATION the counter PRESET COUNT input is taken to a "0" level which loads the true thumbwheel code into the SN74190, e.g. DCBA equals 0011 for a setting of three.

Next, the COUNT DIRECTION input is taken to a "1" level to set the count direction to DOWN, and the START CLOCK input initiates the sequence.

The counter will then count 2, 1, 0, whereupon the MAX/MIN output of the SN74190 will go to "1" clocking BS1 and stopping the clock via G2, only three pulses having been produced in all.

To generate the 10 minus *n* pulses required during DIVISION NORMALISATION the counter is loaded with the same code as before but in this case the count direction is set to UP, and the sequence for the example of three is, 4, 5, 6, 7, 8, 9, 0, producing a total of seven pulses. The D output of the counter is used to trigger BS1 in this case, not the MAX/MIN output.

BOARD OUTPUTS

There are several outputs from the CLOCK board, some of which (such as the A and Z register buffered clock lines), are self-explanatory. Gate G7 is used to detect counts six and seven to give a negative-going edge after clock seven to trigger the counter boards used during MULTIPLICATION and DIVISION. A trigger for this purpose is produced early in the sequence to allow the COUNTER boards and COMPARATOR to register an equality during MULTIPLICATION and still have time to stop the clock at the end of its run.

This output is called PLUS/MINUS COMPLETE. Gate G12 is used to buffer the pulse produced after each batch of ten clock pulses to give the END OF TEN output required by the error detection, or OVERFLOW logic.

The RESTART output is taken from the Q output of BS1 and is used to restart the programme during MULTIPLICATION or DIVISION when the series of additions or subtractions have been completed.

The A register PRESET buffer gates are included on this board for convenience, and have no logic connection with it. They are parallel connected to provide the high drive capability required by the PRESET function of the SN7496.

CONSTRUCTION

This circuit is built on a DL109/22 card, which has a 22-way edge contact on the printed side of the board. The component layout and edge contact wiring is shown in Fig. 7.7.

Wiring-up follows the same pattern as was outlined for previous boards.

The value of the capacitor used to set the clock frequency is about 3,000pF for the completed Digi-Cal (three 0·01μF capacitors in series were used in the prototype) but during testing procedure it is often convenient to use a very slow clock to enable the exact operation of the programme for instance to be traced using only the display and perhaps a voltmeter as indication.

The prototype has been tested with values as high as 1,000μF and still operated correctly, if rather slowly! For this reason it is better not to wire in a capacitor permanently at this stage since a suitable component can be connected when required.

Next month: The Adder Board

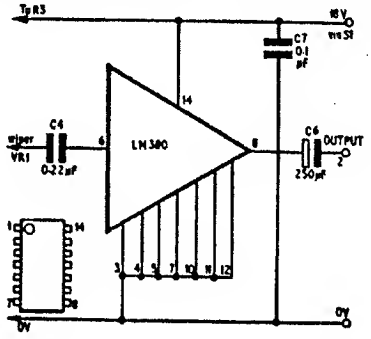
POINTS ARISING

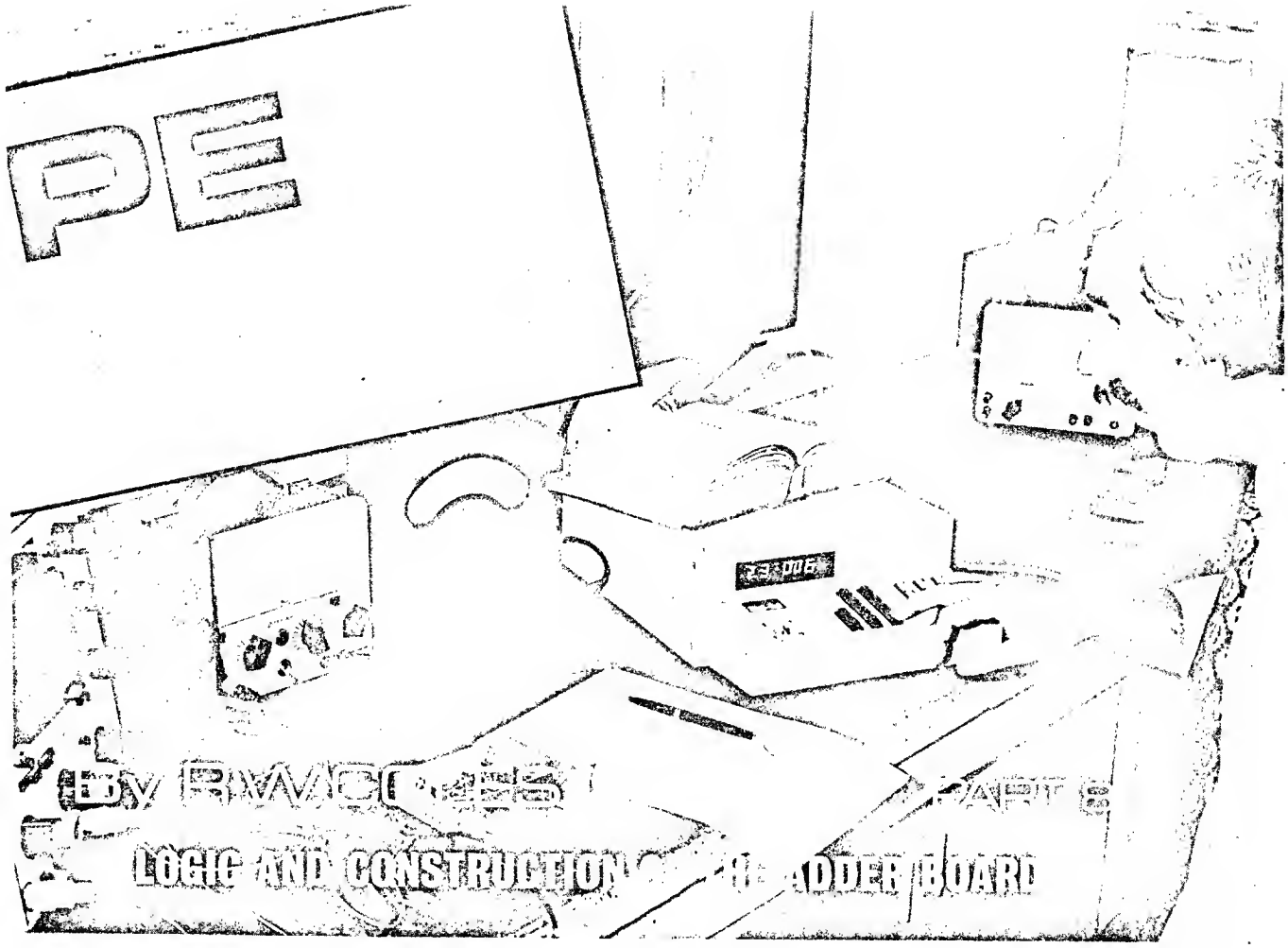
I.C. INTERCOM *(October 1972)*

It has been brought to our notice that the PA234 i.c. is no longer available. A suitable alternative (not substitute) is the LM380, a 2W amplifier with its gain preset at 50. It requires fewer external components than the PA234 (R4, R5, R6, and C5 are not necessary) as shown below.

Minor alterations to the Veroboard layout are required. Pins 3, 4, 5, 10, 11 and 12 must be connected to a heatsink for 2W. It is recommended that a piece of copper be soldered to these pins under the panel if the i.c. is to be used at high power for any length of time. (This i.c. will drive an 8 ohm speaker.)

The LM380 is available (£1·45) from D.T.V. Group Ltd., 126 Hamilton Road, London, S.E.27.





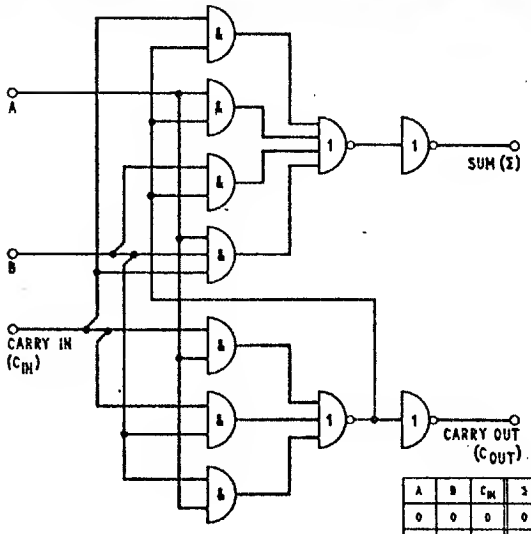
THE BOARD to be described this month is the all important ADDER board which forms the heart of the arithmetic section of the calculator. The name ADDER is a shortened name for what is really an adder/subtractor with carry store, but before going into the design of the board in detail it is necessary to recall some of the principles of binary and B.C.D. addition and subtraction.

BINARY ADDER

The principles involved in a simple single stage binary full-adder are fairly well known in this, the computer age, but for the sake of completeness it is as well to run over them again here.

Fig. 8.1. shows the logic diagram of a typical binary adder which generates a SUM and CARRY output from the three inputs termed A, B, and CARRY IN. The word "typical" is quite meaningful in this connection because a circuit to perform binary addition can be made up in a number of different ways, the end result being the same, no matter which gating arrangement is used.

The performance of this sort of array is best described in terms of a truth-table which lists the circuit's output response to all possible input conditions, and the truth-table for the ADDER is also given in Fig. 8.1. If any reader is unfamiliar with the basic rules of binary addition, studying the truth-table will tell all.



A	B	C_{IN}	Σ	C_{OUT}
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Fig. 8.1. Single binary full adder stage. The truth table defines all the outputs for all combinations of inputs

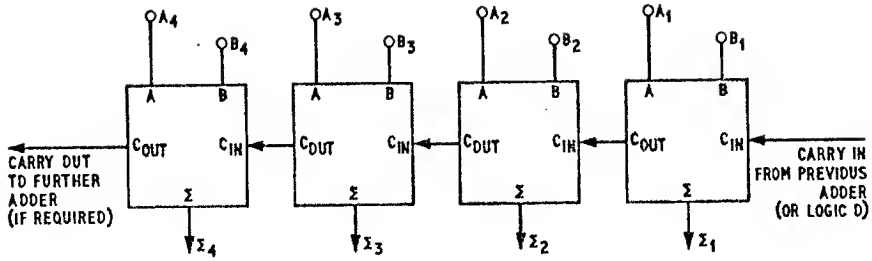


Fig. 8.2. A parallel binary adder to add two four-bit words. Each of the stages in this adder is identical to that shown in Fig. 8.1

PARALLEL BINARY ADDER

A binary adder stage like that of Fig. 8.1 is of limited use as it stands, being capable of adding together only a single pair of binary digits and a carry, whereas most sums a machine is asked to solve would stretch to a number of pairs of such digits. The simplest way to extend the capabilities of this circuit is to use a number together to form a parallel adder like the one in Fig. 8.2.

Each pair of binary digits in the two numbers to be added has its own adder circuit with the CARRY connected in series down the chain. This method of addition is widely used in binary computers but suffers from the disadvantages of large scale component use and slow propagation of the serial carry which has to "ripple-through" to the last stage before the addition is complete.

A circuit arrangement which only uses a single adder stage to add two n-bit numbers is quite possible if the addition is carried out sequentially, i.e. one pair of digits at a time, in a system such as that shown in Fig. 8.3. This method of binary addition is called "serial addition" and requires a store to "remember" the CARRY from a previous addition so that it may be added in with the next.

The two basic addition methods are both employed in Digi-Cal, with some special modifications to allow operation in the B.C.D. code.

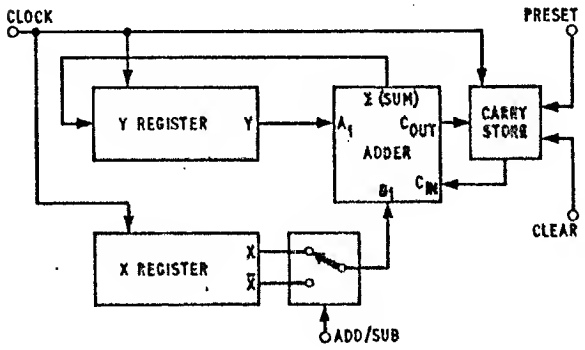


Fig. 8.3. Basic serial binary adder/subtractor. The ADD/SUBTRACT unit presents either the true or complemented output from the X REGISTER to the adder under the control of the FUNCTION CODE A signal

SUBTRACTION

Once the truth table required of a binary subtractor has been worked out it is quite easy to design a simple logic circuit to perform the operations required, but in practice this is very seldom done, because, by making the number to be subtracted negative, i.e. by complementing it, it is possible to achieve the effect of subtraction in an adder circuit of the types already described.

The principles underlying this method of subtraction are quite straightforward and it can be readily appreciated that adding a negative number is the same as subtracting a positive one. Turning a positive binary number into a negative equivalent is simply achieved by inverting all its digits so that all the ones become zeros and vice versa, and then adding a one in the least significant position, for example

binary three	0011
becomes	1100 plus 1
equals	1101

To show that this process does generate a negative equivalent we can add the result to say binary four:

binary four	0100
plus binary thirteen	1101 (complement of binary three)
equals	0001 which is correct

Note that the carry digit from the most significant stage is disregarded, being only an indication of whether the result is positive (as in this case) or negative (if no CARRY results).

The operation of these principles in a practical circuit can be seen in Fig. 8.3 which is a serial adder system with subtraction carried out by simply feeding the inverted version of the X REGISTER output to the ADDER, and arranging for a carry to be preset into the store before the start of the clock pulse series.

M.S.I. ADDERS

The TTL medium scale integration process has been used to produce several different binary adder circuits ranging from the very flexible SN7480 single, full adder to the compact SN7483 circuit which contains four complete adders arranged as a four-bit parallel adder. It is this latter device which is used

in the Digi-Cal adder circuitry, where the four-bit length lends itself well to use with the binary coded decimal (B.C.D.) arithmetic process.

The SN7483 is used as a basic building block in the adder to be described and before venturing into the intricacies of B.C.D. addition and subtraction it is best to become familiar with its construction and operation in its intended role as a parallel binary arithmetic unit.

The equivalent logic circuit of the SN7483 is shown in Fig. 8.4 and comparison of this logic with Figs. 8.1 and 8.2 will show that this device is connected to add together two, four-bit binary numbers with a CARRY IN to the first (least significant) stage, termed C_0, and a carry out from the final (most significant) stage termed C_4.

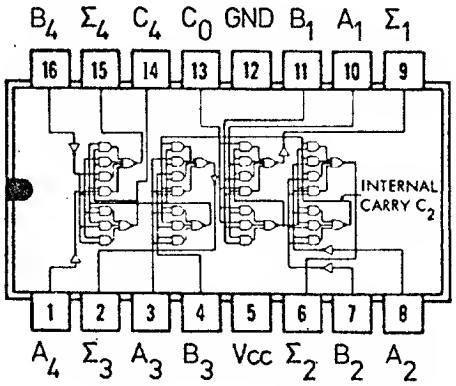


Fig. 8.4. The internal logic of the SN7483 four bit binary adder i.c.

The two four-bit words to be added to indicate the termed A and B with a suffix 1 to 4 to indicate the significance of each bit. The carry circuit delays have been reduced as far as possible by internal connection, the use of high-speed type gating, and the elimination of unnecessary inversion circuitry, so that the addition time is kept below 100ns.

BINARY VERSUS B.C.D.

The numbers stored in the registers of Digi-Cal are represented by groups of four binary digits conforming to the Binary Coded Decimal (B.C.D.) code. This code is not complicated since it is identical to straight binary except that only the values 0 to 9 inclusive are allowed in each four-bit group instead of the values 0 to 15.

With straight binary the word length can be any convenient value, depending on the quantities to be represented, each increment to the word length increasing the range of representable quantities by a factor of two.

In the B.C.D. system however the binary word length must not exceed four bits, and the value of each four-bit word must not exceed 9. Capacity is increased by adding extra four-bit B.C.D. words, each of which increases the range of representable quantities by a factor of ten. As an example of the contrast between the two systems:

0110 equals 6
1001 equals 9 } (In straight binary *or* B.C.D.)

01101001 in straight binary equals 105

0110,1001 in B.C.D. equals 69

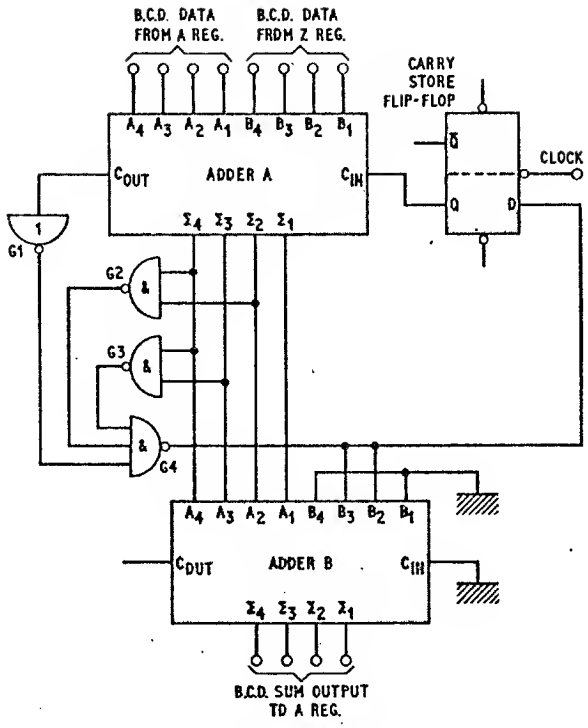


Fig. 8.5. Basic practical B.C.D. adder with a carry store flip-flop

The use of B.C.D. in calculators is desirable because of the simplicity in interfacing the logic with old fashioned human operators who insist on thinking in the decimal number system.

B.C.D. ADDITION

When two four-bit B.C.D. words and a possible B.C.D. carry bit are added together in a parallel binary adder a total of 19 different (four-bit + carry) sums can be produced. Since the largest quantity representable in the B.C.D. code is 9, it is obvious that the nine most significant sums will require correction, and will be responsible for the generation of a B.C.D. carry bit. A moment's thought reveals that the correction required by sums from ten to 19 is the subtraction of ten, e.g.

7 plus 6 equals 13

subtract	10	
equals	3	plus a carry to the next decade.

As we have seen already, the subtraction of ten is readily achieved by adding its complement, which is 0110, or 6 if you prefer, and so the problem reduces to that of detecting sums in excess of nine so that the subtraction can be initiated.

The basic circuit of the B.C.D. adder used in Digi-Cal is shown in Fig. 8.5. Here the two B.C.D. words are added in ADDER A in the conventional binary fashion, the detection for sums in excess of nine being performed by gates G1, 2, 3, and 4. If any such sum is detected G4 feeds a carry to the carry-store

flip-flop and inserts 0110 into ADDER B where it is added to the sum from ADDER A.

The output from the second adder is the correeted versions of sums over ninc, but if a carry is *not* required because the sum is less than or equal to nine, ADDER B passes the sum from ADDER A through to its output in an unmodified form due to the addition of 0000 instead of 0110.

CARRY DETECTION LOGIC

The performance of gates G1, 2, 3 and 4 in detecting sums in excess of nine can bc taken for grantcd if thc rcader prefcrs, but for those who would like to know how the gating arrangement was arrived at, and who have some previous logic experience, the design was carried out as follows.

The CARRY OUT from ADDER A is a ready made indication that the sum is in exeess of 15, which reduces the problem to that of detecting sums of between 10 to 15 inclusive. To determine the gating requircd, the sums in question are plotted on a Karnaugh map, as shown in Fig. 8.6.

The Karnaugh map is just a special way of drawing a truth table to make it easy to see what gating will be required to generate a specific function. It has the property that where adjacencies occur in the plots, thc particular value, or values which change between the plots can be eliminated from the resulting logic equation.

As can be seen in Fig. 8.6 there are two distinct groups of plots, 10, 11, 14, 15, and 12, 14, 15, 13. In thc first group the terms Σ_1 and Σ_3 change, and can be eliminatcd. In the second group the terms Σ_1 and Σ_2 change, resulting in the required gating function of (Σ_2 AND Σ_4 OR Σ_3 AND Σ_4) OR (C_{out}).

This function could be realised using two two-input AND gates and a three-input OR gate, but as the standard gating function of TTL is NAND it is possible to invert C_{out} NAND Σ_2 and Σ_4 and Σ_3 and Σ_4, and feed these inverted functions to a further NAND gate which carries out the NOR function because of the inverted nature of its inputs.

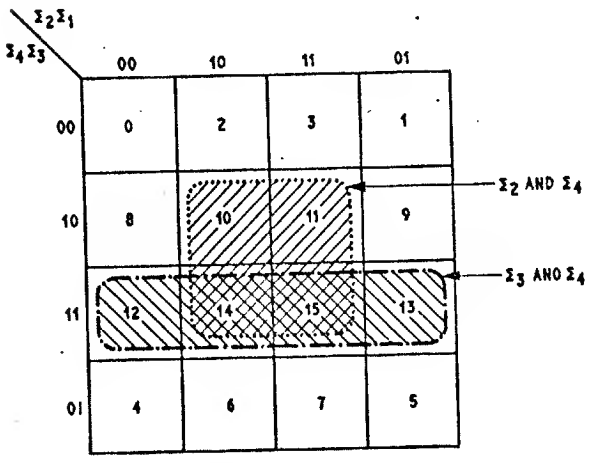


Fig. 8.6. The Karnaugh map used to determine the gating required to detect the sums from 10 to 15 inclusive

B.C.D. SUBTRACTION

The B.C.D. ADDER just described cannot be used for subtraction as it stands, and thc method of addition of complements is complicated by the fact that it is not the straight binary complement which is required, but the decimal complement which can be defined as 10 minus the number to be subtracted. In praetice the gencration of the "tcns complement" causes problems with thc carry logic, and it is preferablc to generate the "nines complement" by subtracting from nine and then use thc carry logic to add in a 1.

The gencration of the "nines complement" of the data from the Z REGISTER requires thc addition of the circuit shown in Fig. 8.7, which employs yet anothcr SN7483 quad adder.

The principle behind this "nines complementer" is that the binary complement of the input data is added to binary nine to produce nine minus z, but since the binary complement of a number is its inverted version plus 1, in practice the circuit adds the inverted z data to binary 10 thus taking care of the extra 1 required by the complement.

The inversion of the z data is carried out in an SN7486 quad exclusive-OR gate, which, when connected as shown, allows a true version of the input data through to the output when the common control input is a logic 0, and an inverted version when the control is a logic 1.

This useful property of exclusive-OR gates, along with the fact that it is the control input which inserts the required 1010 into the adder, allows the "nines complementer" to either pass the z data unmodified when FUNCTION CODE A is a logic 0 indicating an addition is required, or pass the "nines complement" of the z data when the FUNCTION CODE A line is a logic 1 indicating that subtraction is required.

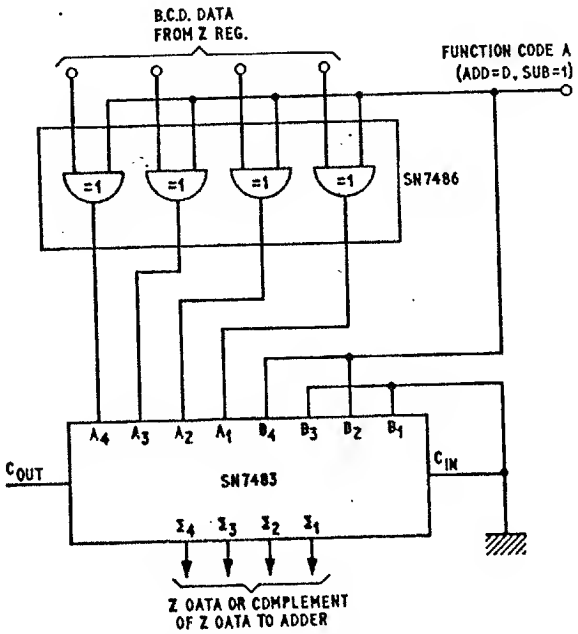


Fig. 8.7. B.C.D. nines complementer. This generates the output 9 minus Z when subtraction is required

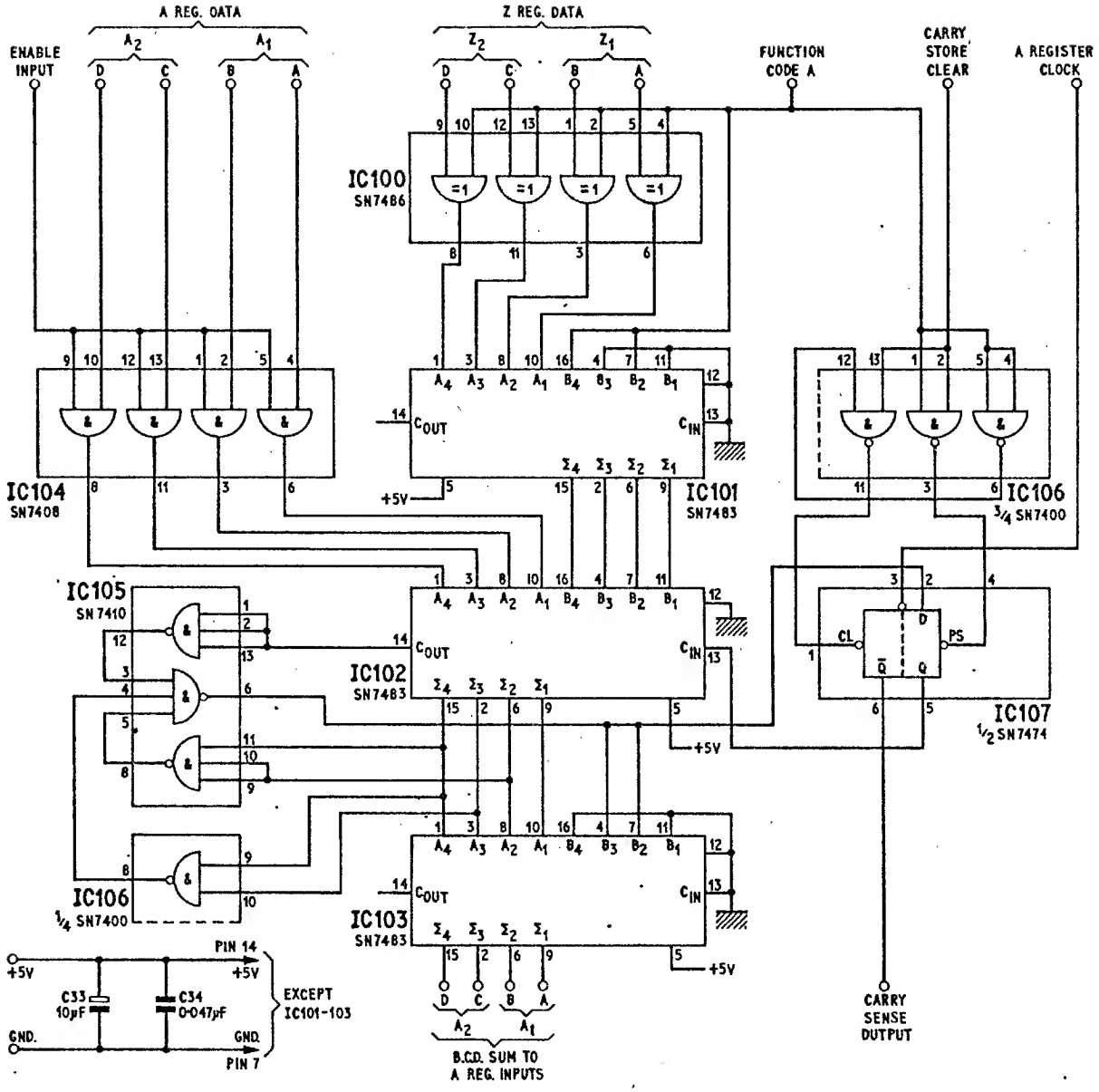


Fig. 8.8. Complete circuit diagram of the ADDER board

The details of the subtraction process are quite hard to grasp at first but the process may be easier to understand after working through the following example (right).

Note that the borrow function which would be generated if the answer to a subtraction is negative is stored in the carry store in the opposite sense to that of a carry in addition, i.e. a 1 stored means no borrow, and vice versa.

FULL CIRCUIT DIAGRAM

The complete circuit of the Digi-Cal adder/subtractor is shown in Fig. 8.8. This circuit is made up of a combination of the ADDER and COMPLEMENTER circuits already covered, with the addition of IC104 and gating for the CARRY STORE PRESET/CLEAR input.

A Register data	1000	(equals 8)
B Register data	0110	(equals 6)
Carry store	1	No borrow from previous subtraction
Function Code A	1	Subtraction
START ADDITION		
Invert Z data	1001	
Add to 1010	0011	
Add to A data plus carry input	1100	B.C.D. carry generated
Add 0110	0010	Equals 2, the required answer

COMPONENTS

ADDER BOARD

Capacitors
C33 10μF 15V elect.
C34 0·047μF

Integrated Circuits
IC100 SN7486
IC101–IC103 SN7483 (3 off)
IC104 SN7408
IC105 SN7410
IC106 SN7400
IC107 SN7474

Printed Circuit Board
Type DL109/22 (Shirehall)

IC104 is an SN7408 quad AND gate which is connected as an A REGISTER data inhibit, requiring its common ENABLE input to be a logic 1 before the A data is allowed through to the ADDER.

The purpose of this i.c. is to allow flexibility in the programming possibilities and, particularly, to inhibit data recirculation when the A REGISTER data is being normalised after a multiplication sequence.

The normalisation process was covered last month, and readers may recall that after multiplication, the A data are shifted to the right by the number of decimal places selected on the thumbwheel.

If the inhibit gates were not fitted the data which were to be discarded during normalisation would recirculate and appear at the most significant end of the A REGISTER. The ENABLE input is controlled by the programme.

The purpose of the gating in the CARRY STORE PRESET and CLEAR inputs is to allow for the fact that a BORROW is stored in the opposite sense to a CARRY, requiring the store to be preset before a subtraction, and cleared before an addition. Since there is a single CARRY STORE CLEAR signal from the programme, the FUNCTION CODE A input is used to control two, two-input NAND gates which steer the CLEAR signal to the correct side of the CARRY STORE flip-flop.

The only other part of the circuit worthy of note is the CARRY SENSE output which is used to inform other parts of Digi-Cal of the state of the CARRY STORE, one of its uses being to stop subtractions when a BORROW is produced after any tenth clock pulse during division, i.e. it senses when the A REGISTER contents are negative.

CONSTRUCTION

The construction and wiring of the ADDER board is quite straightforward since the circuit is housed on the usual Dualine card, in this case a DL109/22.

On this board almost all of the connections are carrying high speed data signals which must have a high integrity, and for this reason it is necessary to keep wiring as short as possible to minimise problems caused by line reflection.

The component layout and edge connector wiring is shown in Figs. 8.9 and 8.10.

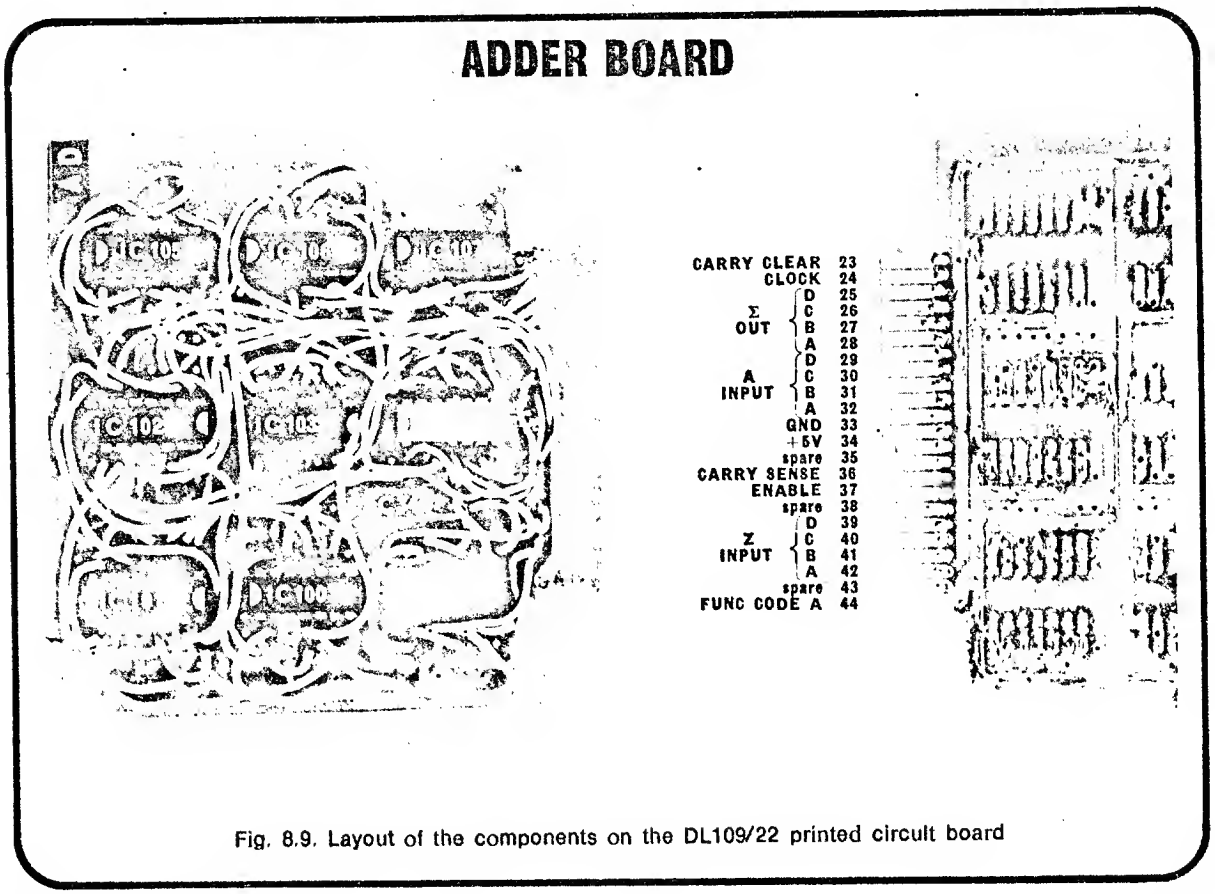


Fig. 8.9. Layout of the components on the DL109/22 printed circuit board

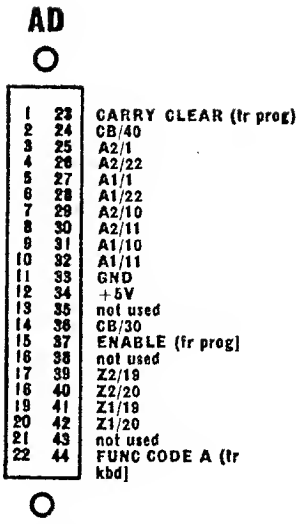


Fig. 8.10. Function of the edge contacts for the ADDER board

TESTING

Checking out this board in isolation is relatively easy since it is possible to check the sum responses to various dummy control and data inputs. The data values can be inserted by wiring each of the four data lines from the separate sources to ground, or leaving them open circuit, to simulate a particular B.C.D. number.

Providing the ENABLE and FUNCTION CODE A lines are also properly activated, a B.C.D. answer should appear on the SUM outputs from IC103, and a CARRY/BORROW signal at the D input of IC107. The CARRY STORE CLEAR input can also be tested in combination with FUNCTION CODE A, monitoring the result at the Q or $\overline{Q}$ output of the flip-flop.

Constructors who have followed the assembly sequence suggested will also be able to try the first complete calculations on their machine by judicious application of dummy control signals which would normally emanate from the programme.

Numbers entered into the ENTRY REGISTER can be transferred to the Z REGISTER by operation of the (cleared) A REGISTER by momentarily grounding the START CLOCK input to board CB. This process requires a large number of temporary control signals to be wired in, and may be daunting to some readers: the prospect has been suggested only to enable the more adventurous to experiment with the way the programme board (to be described next month) will be required to carry out the process of addition and subtraction automatically. Those who do attempt this type of test will learn a great deal about the intimate workings of Digi-Cal.

Note: In Part 4 (Oct. 72), Fig. 4.2, C13 on IC21 should be marked C9, and C8 should be 10μF not 22μF

Next month: Programme Board

NEWS BRIEFS

COMPUTER '72

TAKING both the Grand and National Halls at Olympia, the COMPUTER '72 exhibition (December 4 to 8) attracted over 200 international companies who had data processing services to offer. The organisers of this show, the Business Equipment Trade Association, described its purpose as "explaining the benefits of electronic data processing to commercial and industrial management", thus the exhibition presented services rather than the actual hardware itself, though peripherals were much in evidence.

One of the most attractive stands was that of the Post Office. The display was a symbolic representation of their Datel services in multicoloured plastics, with some exhibits showing data transmission techniques of the past.

On the hardware side, Hewlett-Packard presented their new minicomputer, Model 30. This computer is no larger than a good sized teletype terminal and provides an economical alternative to time-sharing, operating in BASIC, the language most used for time-shared systems. It has an internal cassette store with a capacity of 24,000 numbers. Its readout is via an 80 character alphanumeric display, though a printer is an optional extra.

As well as the main exhibition some light relief was provided by Honeywell who presented the winning entries to the Observer Colour Magazine children's "Paint-a-Computer" competition. Also on display was the Honeywell/Roland Emett forget-me-not computer. On the NCR stand a simulated game of cricket was being played through one of their computers and results were presented as the "game" progressed.

The bringing together of a large nuumber of companies in this way is obviously a great service to management and the success of this and future shows is assured.

High Speed Printer Using a Laser

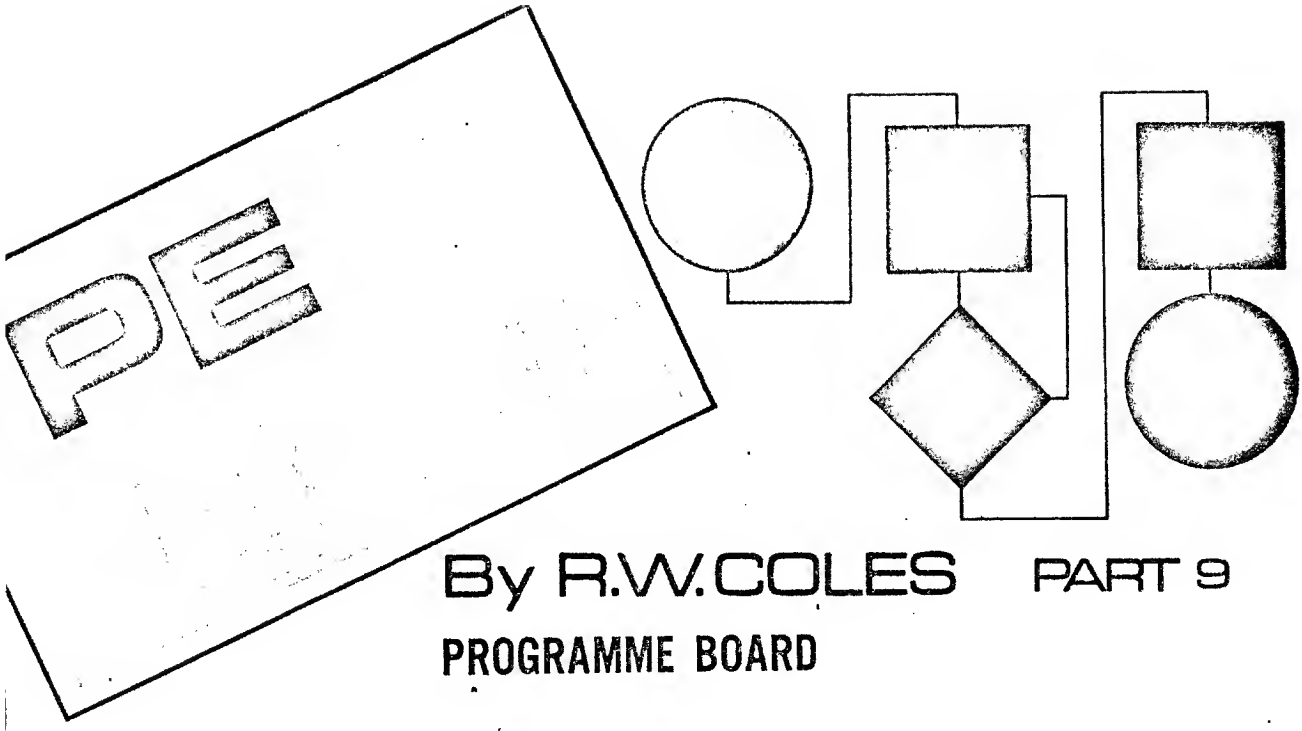
A NON-IPACT printer capable of writing 1,000 lines per minute is being developed by R.C.A. for the U.S. Army. The new printer uses a laser to transfer digital communications alphanumerics onto ordinary paper.

The printer is called the Material Transfer Recorder (MTR) and uses a dye-coated plastic ribbon scanned by the laser beam to record the messages on the ordinary paper.

There are no keys as in normal mechanical printers thus wear problems and maintenance are greatly reduced. Also the printer is almost silent because of the lack of impact.

Through its data interface the MTR can receive any type of digital signal from a wide varicty of sources including satellite ground terminals. It can receive this information at the rate of 20,000 words per minute.

The MTR is easily transportable and can be used in the field in a van or any other military shelter.



By R.W.COLES PART 9

PROGRAMME BOARD

THE BULK of the Digi-Cal logic has now been described. Throughout the articles covering the logic boards from DISPLAY to ADDER, readers will constantly have encountered a variety of signals attributed to a mysterious PROGRAMME BOARD.

The far-reaching influences of this board thus having been established, the time has arrived to delve into the method of deriving the plethora of programme output signals, a most important aspect of the calculator.

DIGI-CAL PROGRAMME

The requirements of Digi-Cal are humble, re-programming not being required in the normal run of things and the tasks for which a programme is necessary, namely the four arithmetic functions of addition, subtraction, multiplication and division can be carried out with only a few programme steps and without recourse to any high level language facilities other than the press of an appropriate key.

Programming then is carried out at the basic level of logic gates and flip-flops, and the Digi-Cal philosophy is retained by making the programmes variable by wiring in diodes where required in a matrix arrangement.

The separate jobs to be controlled by the programme include shifts, transfers, register and counter clearing, routing and clock pulse initiation, all of which must be carried out in a strict sequence.

PRINCIPLES OF PROGRAMME GENERATION

The programmes for Digi-Cal are formed in a diode matrix in the form of a Read Only Memory or R.O.M. "Memory" because a number of separate addressable locations are provided, and "Read Only" because the instruction data in each address location is fixed at the wiring-up level and is not altered by the operator.

In the present system the R.O.M. array is addressed sequentially by means of a counter. In this way each location in the memory is addressed in turn starting each time at address "1" and continuing to the final address of each R.O.M. in an incremental fashion.

It is not possible to jump back or forward in the sequence and random addressing of a particular location is likewise impossible.

Pausing during a sequence for an indefinite length of time is possible, as is aborting the sequence by clearing the address counter and stopping the clock.

BASIC CIRCUIT

The incremental ADDRESS COUNTER/R.O.M. programme system is best understood initially by means of a simplified circuit without any trimmings (Fig. 9.1).

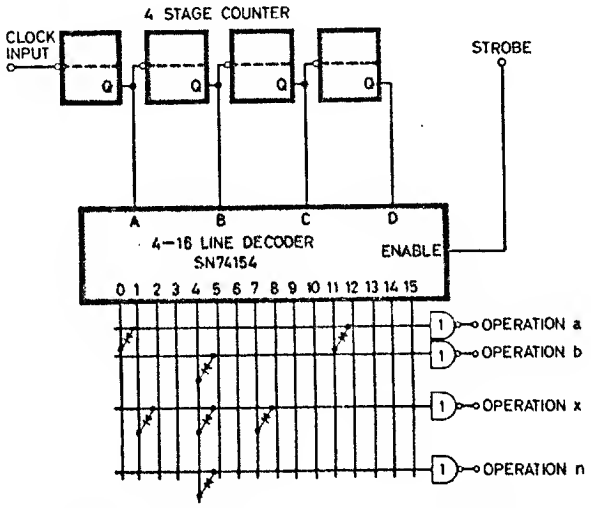


Fig. 9.1. Principles of Read Only Memory Programme generation

Here, a four stage binary counter with 16 possible states is driven continuously by a clock pulse train. The system states of the counter are individually decoded by gates which produce an active low output when inputs are in the appropriate states.

These gates are in the form of an SN74154 TTL M.S.I. decoder which has extra facilities to generate the complement versions of the four inputs required by the decoder gates and a common overriding enable, or strobe input which can be used to inhibit all outputs.

The pin connections of the SN74154 is shown in Fig. 9.2. Referring again to Fig. 9.1 with Fig. 9.2 in mind, it can be seen that, as the counter steps through the sequence, each output from the decoder is enabled in turn for one clock period, thus establishing the programme steps.

The number of operations to be controlled by the programme depends on the requirements of the machine controlled, and can be few or many as required only four being shown in the basic circuit.

All that remains to perform a particular operation in a particular programme step, is to connect a diode across the appropriate intersection where the step line crosses the operation line.

DIODE MATRIX

Inverters are used at the output end of the operation lines to act as what could be described as "sense amplifiers" in traditional memory terms. Another way of looking at the operation lines and inverters is as multi-input NOR gates with the number of inputs to each gate being determined by the number of times that an operation is used.

Note that each operation can be used any number of times and also that any number of different operations can be activated simultaneously.

The basic circuit has no facilities for stopping or starting the sequence which therefore runs continuously. Also only one programme is catered for and, because of the ripple-through counter circuit propagation delays combine to give spurious pulses of a few nanoseconds width on some of the step lines.

All of these disadvantages have to be overcome in the Digi-Cal circuit, which is shown in Fig. 9.3.

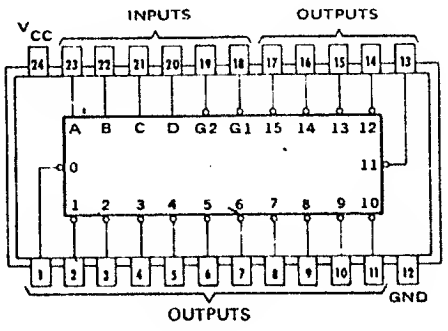


Fig. 9.2. The pin connections of the SN74154 four line to 16 line decoder

FULL CIRCUIT

The full circuit looks very much more complicated at first sight but the R.O.M. arrays can be easily identified, and the rest of the tangle breaks up into sections with specific jobs.

First out of the way are IC108, 109 and 110 which are simply there to divide the master (ungated) clock signal from board CB by a factor of a thousand, to allow the programme circuits to operate at slow speed.

This eases reflection and decoding problems while keeping the operation of the calculator logic tied to a master synchronising clock signal. The only special thing about these dividers is the fact that the three SN7490 are connected in the $\div 10$ mode which gives a 1 : 1 mark space output from the final stage.

This is arranged by connecting the A stage of the circuit after the B, C, D stage.

STOPPING AND STARTING

An SN7493 (IC112) is used as the programme counter, and it is made to stop or start counting by means of a gate in its clock line. Gate G1 itself is controlled by a latch flip-flop which is SET by a pulse from the EQUALS key monostable in the keyboard logic and RESET by the programmes themselves.

Setting the latch is accomplished by using the clock input with a permanent "1" on the D input and clearing is achieved by using the programme STOP PROGRAMME operation to energise the CLEAR input of the first flip-flop via a monostable formed from the other flip-flop and a couple of inverters.

This method of forming a monostable was described in the article covering the CLOCK BOARD, Fig. 7.5, a monostable being necessary in this case to prevent "race" conditions removing the RESET input before the latch was properly cleared.

PROGRAMME SELECTION

Three separate programmes are required in Digi-Cal; three rather than four because the sequences for ADDITION and SUBTRACTION are identical, the distinction being drawn by the fact that the ADDER BOARD operates either as a subtractor or an adder depending on the FUNCTION CODE which is produced directly by keyboard depressions.

The ADD/SUBTRACT programme is quite simple as might be expected and requires only a few steps. Seven steps are, however, provided to allow reprogramming if any "frills" such as round-off or true negative answer are considered possible later.

The MULTIPLY and DIVIDE programmes are separate and have a possible 15 steps each, to allow for the increased complexity of these operations. Some spare steps are also left in these operations, and can be employed as required.

The selection of the required programme is accomplished by utilising the G1/G2 ENABLE inputs on the SN74154 decoders providing the MULTIPLY and DIVIDE sequences, and by using the D input for the same purpose on the SN7442 of the shorter ADD/SUBTRACT sequence.

Using the D input as an enable is possible with the SN7442 because if the D input is high, the output selected must be greater than seven and since only outputs one to seven are used, a high D input means all programme steps are disabled even though they may be addressed by the A, B and C counter outputs.

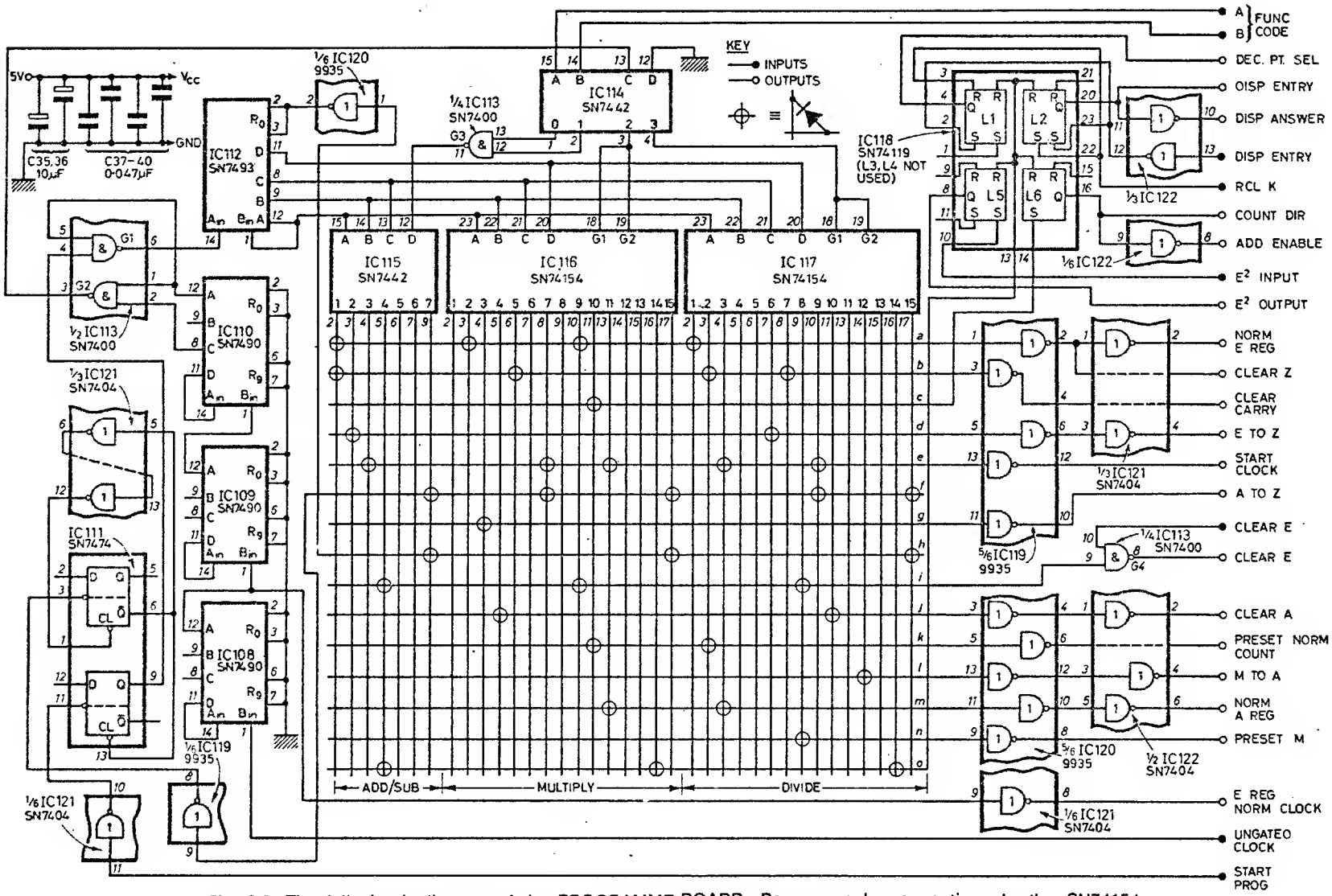


Fig. 9.3. The full circuit diagram of the PROGRAMME BOARD. Power supply connections to the SN74154 and SN74119 are shown in Figs. 9.2 and 9.6. All others have V_{CC} to pin 14 and GND to pin 7 except the SN7490 and SN7493 which has V_{CC} to pin 5 and GND to pin 10, and SN7442 which has V_{CC} to pin 16 and GND to pin 8

COMPONENTS

Capacitors
C35, C36 10μF 15V elect. (2 off)
C37–C40 0·047μF (4 off)

Diodes
D104–D142 West Hyde type "red" (or any small silicon diode) (39 off)

Integrated Circuits
IC108–IC110 SN7490 (3 off)
IC111 SN7474
IC112 SN7493
IC113 SN7400
IC114, IC115 SN7442 (2 off)
IC116, IC117 SN74154 (2 off)
IC118 SN74119
IC119, IC120 DTL9935 (2 off)
IC121, IC122 SN7404 (2 off)

Printed Circuit Board
0·1in Veroboard (8·2in × 3·4in)

Edge Connector
32 way 0·1in pitch edge connector (optional)

STROBE SYSTEM

Enabling the appropriate programme decoder is not done in a d.c. manner, with a constant input throughout a particular sequence but in an a.c. manner by routing enabling or "strobe" pulses to the selected decoder which occur in the centre of each addressing period.

This scheme is used to kill two birds with one stone, since by enabling decoder outputs only in the middle of each address period the problem of spurious outputs or "glitches" is overcome.

By the time the enable pulse arrives the address counter is resting in a particular state and propagation delay problems are overcome.

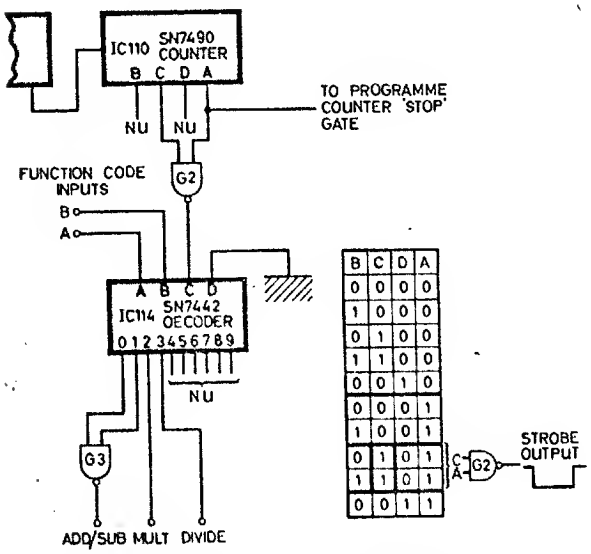


Fig. 9.4. Gate G2 is used to generate a strobe pulse by detecting simultaneous C and A outputs during the clock period as shown in the truth table. The decoder is used to select the appropriate part of the programme according to the FUNCTION CODE inputs

This selection system involves IC114, G2 and G3 and to make the principle clearer it is redrawn in an integrated way as Fig. 9.4. Two states of the final divider (IC110), count sequence are detected by gate G2 which gives a negative strobe pulse near the end of the run (see Truth Table).

The strobe pulse is applied to the c input of IC114 which is being under-used in this application as a two to four line decoder with strobe input.

One of the outputs zero to three is addressed by the two line FUNCTION CODE generated by the KEYBOARD in response to the arithmetic selection made by the operator.

The selected output will remain high however, until the strobe pulse takes the c input low. The result of all this is that a continuous stream of strobe pulses is delivered, via the logic described, to the STROBE or ENABLE input of the selected programme decoder. Gate G3 is used as a negative logic NOR gate to ENABLE the single ADD/SUBTRACT programme whether addition or subtraction is called.

PROGRAMME OUTPUTS

Fifteen programme operations are possible on this board, and although more of these would be useful, board space is a limiting factor for the layout of the R.O.M. matrix.

Because of this limited number of available lines, some outputs do two or more jobs which seem to be unconnected. For example, line A is responsible for normalising the entry register, clearing the Z REGISTER, and clearing the EQUALS LATCH on the M COUNTER boards.

PROGRAMME OPERATION CODE ASSIGNATIONS

a Normalise Entry Register
Clear Z Register
Clear M Counter Equals Latch

b Clear Carry Store
Clear M Counter (to 000000)

c Set latch, changing clock count to DOWN and disabling A inputs to ADDER

d Transfer the contents of the E register to the Z register

e Start Arithmetic Clock

f Stop programme sequence

g Transfer the contents of the A register to the Z register

h Clear the Programme Counter

i Clear E register

j Clear A register

k Preset NORM code from the thumbwheel into the clock counter

l Transfer contents of M counter to A register

m A register NORM in progress

n Preset M counter to 999999

o Clear latch array/select A register for display with point position determined by thumbwheel

These operations are not related and are grouped together because they do not interfere with each other if performed at the same time.

It must be remembered, however, that if a CLEAR Z signal is required by a programme, the other signals are also produced which may or may not be important if a "home-made" programme sequence is employed.

Programme outputs are arranged to be either "active high" or "active low" depending on the requirements of the logic they drive, and for this reason either one or two inverters are placed at the end of the operation lines.

The inverters connected directly to the R.O.M. lines are from the DTL family and are type 935 which do not have input diodes (Fig. 9.5). This enables the R.O.M. diodes to be used as an integral part of the circuit without reducing noise immunity.

LATCH ARRAY

The latch array performs a variety of jobs which are related to the programme, one of the most obvious of which is to stretch programme operations over a number of steps.

"Stretching" is achieved by using the programme to SET a latch in a particular step, and to RESET it in another. The latch output is then used to control a particular operation which must be continued for longer than one step.

Latch L6 is used in this way to control the CLOCK COUNTER direction and ADDER ENABLE during A REGISTER NORMALISATION in the MULTIPLY sequence. Latch L5 is used to control routing logic during an E^2 operation, being SET by pressing the E^2 key and RESET by the CLEAR LATCH ARRAY programme operation at the end of each sequence.

Latches L3 and L4 are not used, but are available if required, and L1 and L2 operate together to control the display selection.

Latch L1 controls the decimal point selection (fixed or floating) and L2 controls the register selection (A or E).

The i.c. used in this position is the very versatile SN74119, which like the SN74154 decoders is housed in a 24 pin dual-in-line package. The logic of this device is simply that of six cross-coupled gate latches with a common clear line, and is shown in Fig. 9.6.

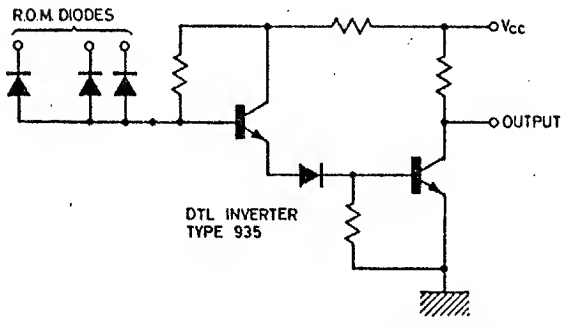


Fig. 9.5. This diagram shows how the R.O.M. diodes and the DTL inverters are used to form NOR gates

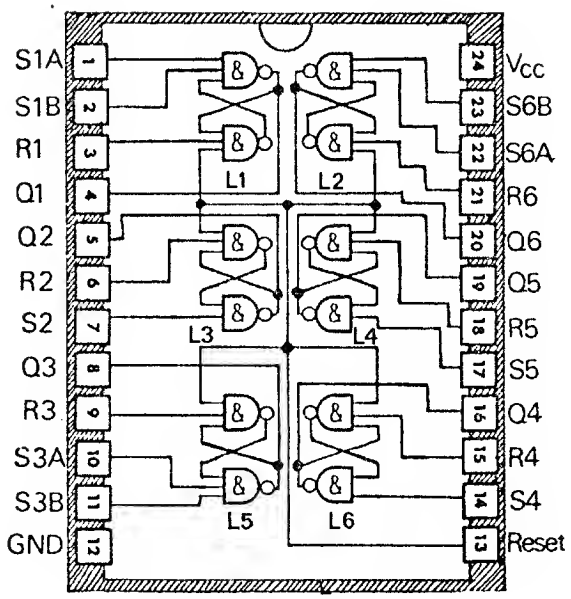


Fig. 9.6. Internal logic of the SN74119 hex SET/RESET LATCH

CLOCK AND CLEAR

There are only a couple of items left on the full circuit to be mentioned, the first of these being G4 which is used to NOR the CLEAR E output from the programme and the CLEAR E input from the CE key to give a combined signal.

Next, the E REGISTER normalising clock output is taken as a tapping from the divider-chain so that although much faster than the final programme clock, the normalising clock is slower than the arithmetic clock to prevent difficulties with the long line lengths used.

PROGRAMMING

The programmes used in the prototype are shown in Fig. 9.7, which presents the sequences as flow diagrams.

The operations inside the shaded boxes in the MULTIPLICATION and DIVISION programmes show the conditional branching operation carried out by the CLOCK GENERATING BOARD, and are included in the flow diagram for completeness.

Each of the square boxes corresponds to the programme step with which it is numbered, several operations being possible at each step. The spare steps do not give rise to any outputs from the board, but may be used to advantage if the basic programme is expanded or re-arranged.

Re-programming does not require any particular skill other than commonsense and a knowledge of the way the circuits operate.

The writer has had very little time to consider just what improvements could be programmed into the calculator, but with a little ingenuity and perhaps modification, true negative answers (as opposed to complement versions as the machine stands) should be possible.

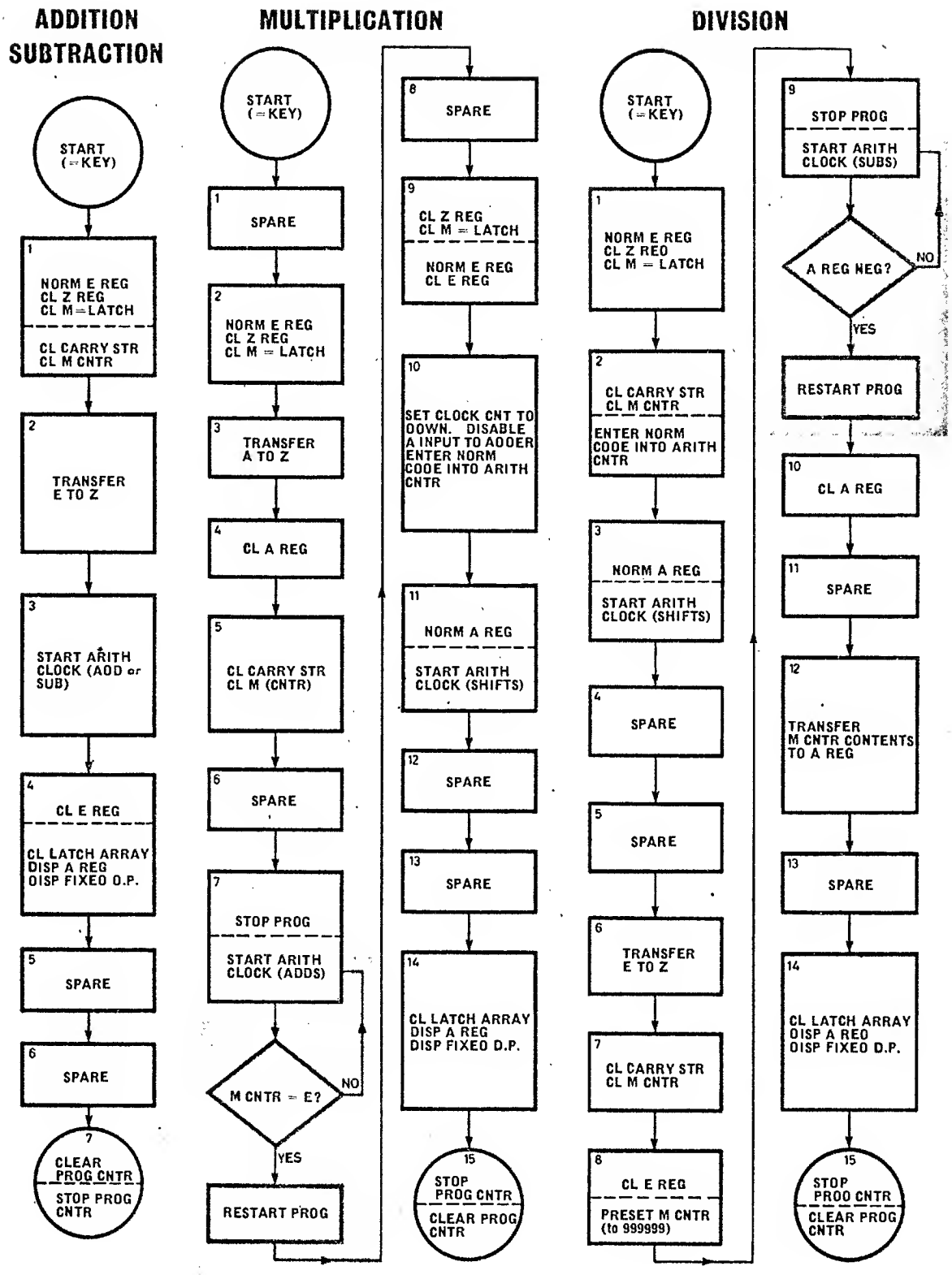


Fig. 9.7. This flow diagram shows the three programmes used on the PROGRAMME BOARD. The same programme is used for addition and subtraction as mentioned in the text

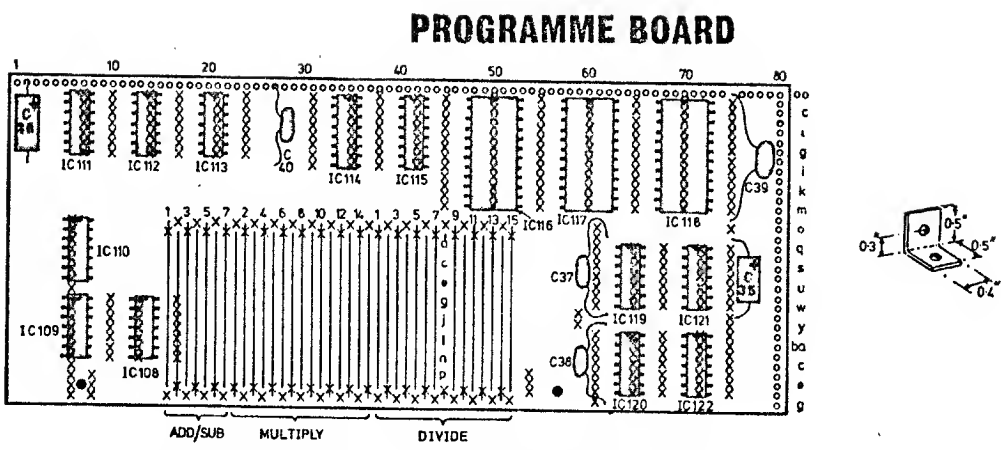
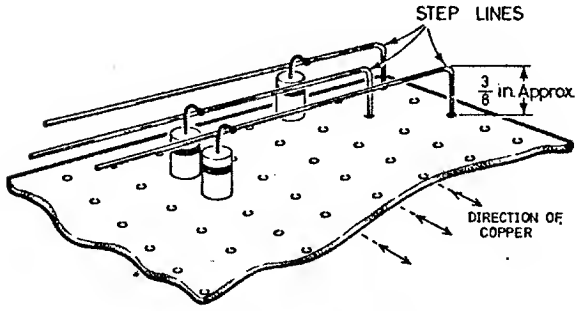


Fig. 9.8. The layout of the components on the Veroboard panel. Crosses show breaks in copper strips



Diode matrix construction

PROGRAMME BOARD WIRING DESTINATIONS

aa	not used
ab	START PROG (fr kbd)
ac	RECALL K (fr kbd)
ad	UNGATED CLK IN (fr CB/43)
ae	FUNC CODE A (fr kbd)
af	DISP E (to disp)
ag	E^2 (fr kbd)
ah	DISP E (fr kbd)
ai	FUNC CODE B (fr kbd)
aj	CNT DIR'N (to CB/28)
ak	CLEAR E (to ED/2)
al	CLEAR E (fr kbd)
am	not used
an	GND
ao	E^2 (to E^2 logic)
ap	+5V
aq	CLEAR Z REG etc (to Z2/43, kbd (NORM) and M1/19)
ar	CLEAR CARRY etc (to AD/23, M1/20, M2/20)
as	DISP A (to DISP)
at	START CLK (to CB/44)
au	not used
av	DEC PT SEL'N (to kbd)
aw	TRANSFER E TO Z (to Z1/24)
ax	E REG NORM CLK (to kbd)
ay	ADD ENABLE (to AD/37)
az	NORM A REG (to CB/37)
ba	PRESET NORM CNT (to CB/27)
bb	TRANSFER M TO A (to CB/39)
bc	not used
bd	PRESET M (to M1/21, M2/21)
be	CLEAR A REG (to A1/44, A2/44)
bf	TRANSFER A TO Z (to Z2/24)

CONSTRUCTION

This circuit is built on a Veroboard panel (Fig. 9.8) and carries a good deal of wiring on both sides. The R.O.M. operation lines are formed by the printed tracks on the board, but the step lines are formed from bare tinned copper wire running at right-angles to the tracks.

These are spaced from the board by about $\frac{3}{8}$in so that diodes may be soldered-in where required. Note that the diodes are inserted with their red ends uppermost, connected to the step lines.

Wiring is congested but not critical, thanks to the low programme speed, and both sides of the board carry wire interconnections.

An edge connector of 32 or more ways is recommended for use with this board, but it is not essential; connections can be soldered directly to the printed tracks if desired. If an edge connector is used it is necessary to clean the track ends thoroughly with fine emery paper and then coat them with a tarnish preventer and cleaner such as Electrolube.

TESTING

Programme selection and step sequences can be easily checked after construction by using a large value capacitor on the CLOCK BOARD to give a very slow programme sequence. Steps can then be followed with a multimeter set to a low voltage range.

Operational testing can be carried out only with the ADD/SUBTRACT programme until the M COUNTER boards and E^2 logic are constructed, but when this is working, little trouble should be experienced with the other programmes.

Note: In Fig. 6.10 (Dec. 72) Z1/22, Z1/43, Z2/22, and Z2/43 go to Z2/44 not CB/13. Z1/21, Z2/21 go to CB/23. A1/42, A2/42 go to CB/40. A1/43, A2/43 go to CB/38. In Fig. 7.7 (Jan. 73) CB/40 should go to A1/42, A2/42.

Next month: M Counter Boards

BY R.W.COLES

PART 10

M COUNTER BOARDS

THIS month's article deals with the M(COUNTER) boards which are the last of the arithmetic unit plug-in cards to be described.

M COUNTER FUNCTION

The basic system used to enable the MULTIPLICATION and DIVISION operations to be carried out was described in Part 1, where it was mentioned that the successive additions and subtractions carried out were counted in a counter circuit.

It is this counter which is housed on the two identical M boards, together with the COMPARATOR circuit required during MULTIPLICATION to register an equality between the count and the contents of the E REGISTER.

BLOCK DIAGRAM

A block diagram of the COUNTER/COMPARATOR circuits and their related data paths is shown in Fig. 10.1, which can be placed in context by reference to the overall system block diagram, Fig. 1.3 of Part 1.

The counter itself consists of a serial string of six, four-bit, decade counter units which have a maximum count capacity of 999999.

The COUNTER can be cleared or preset by appropriate control signals from the programme, and is triggered by the PLUS/MINUS COMPLETE signal from board CB, which is produced during each addition and subtraction.

The six, four-bit, B.C.D. outputs from the counter are fed to the comparator circuit and also to the A REGISTER into which they can be entered at the end of a DIVISION sequence as required.

When the COMPARATOR registers an equality between the count and the E REGISTER contents during a multiplication, it sets a latch which produces the COMPARATOR EQUAL signal, which in turn stops the arithmetic clock.

Before a MULTIPLICATION sequence, the EQUALS LATCH is cleared by a signal from the PROGRAMME.

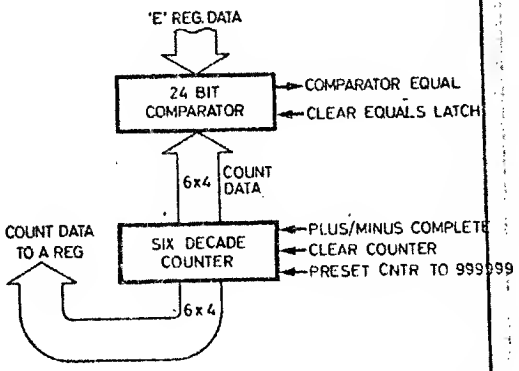
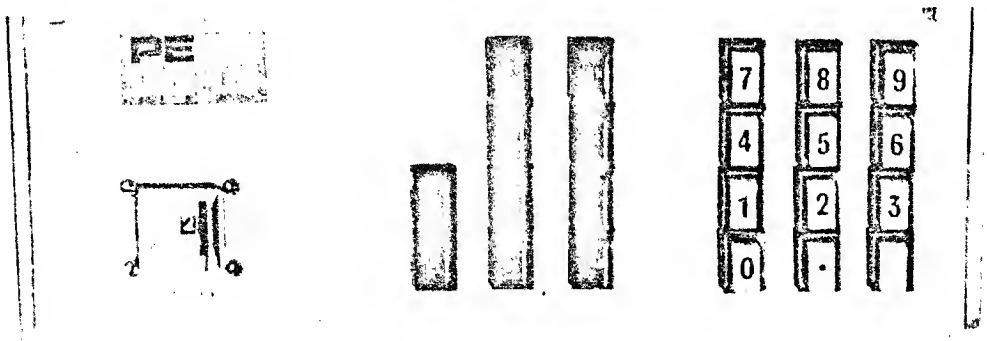


Fig. 10.1. Block diagram of the COUNTER/COMPARATOR circuits and their related data paths



PARTITIONING

A six decade counter and comparator requires too many i.c.s, even when using M.S.I. devices, for it to be housed on a single DL109 card, so the circuit is split into two identical sections, each comprising a three decade counter and a commensurate amount of comparator circuitry. This is described more fully in Fig. 10.2.

Only one EQUALS LATCH is required, but in practice a latch is incorporated on each board to ensure interchangeability, which is an advantage in fault finding, and initial testing.

The latch in use is determined by the external edge connector wiring, no connection being made to the latch inputs and outputs on the board in the M2 position.

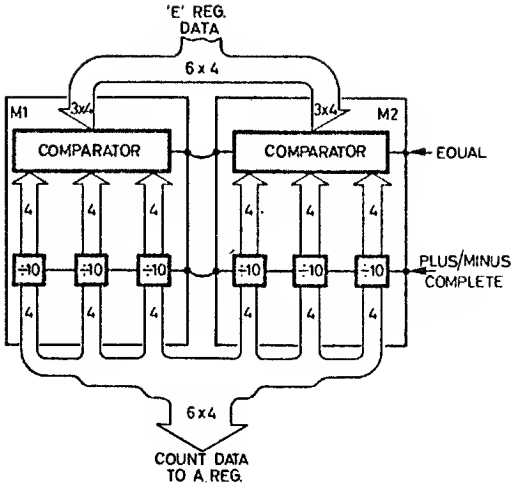


Fig. 10.2. Partitioning of the COUNTER/COMPARATOR between the two M boards

FULL CIRCUIT

The full circuit of one of the M COUNTER boards is shown in Fig. 10.3. The counter chain is easily identified as IC's 123, 124 and 125 which are SN7490 devices connected to count in a B.C.D. code by connection on the A output to the B input.

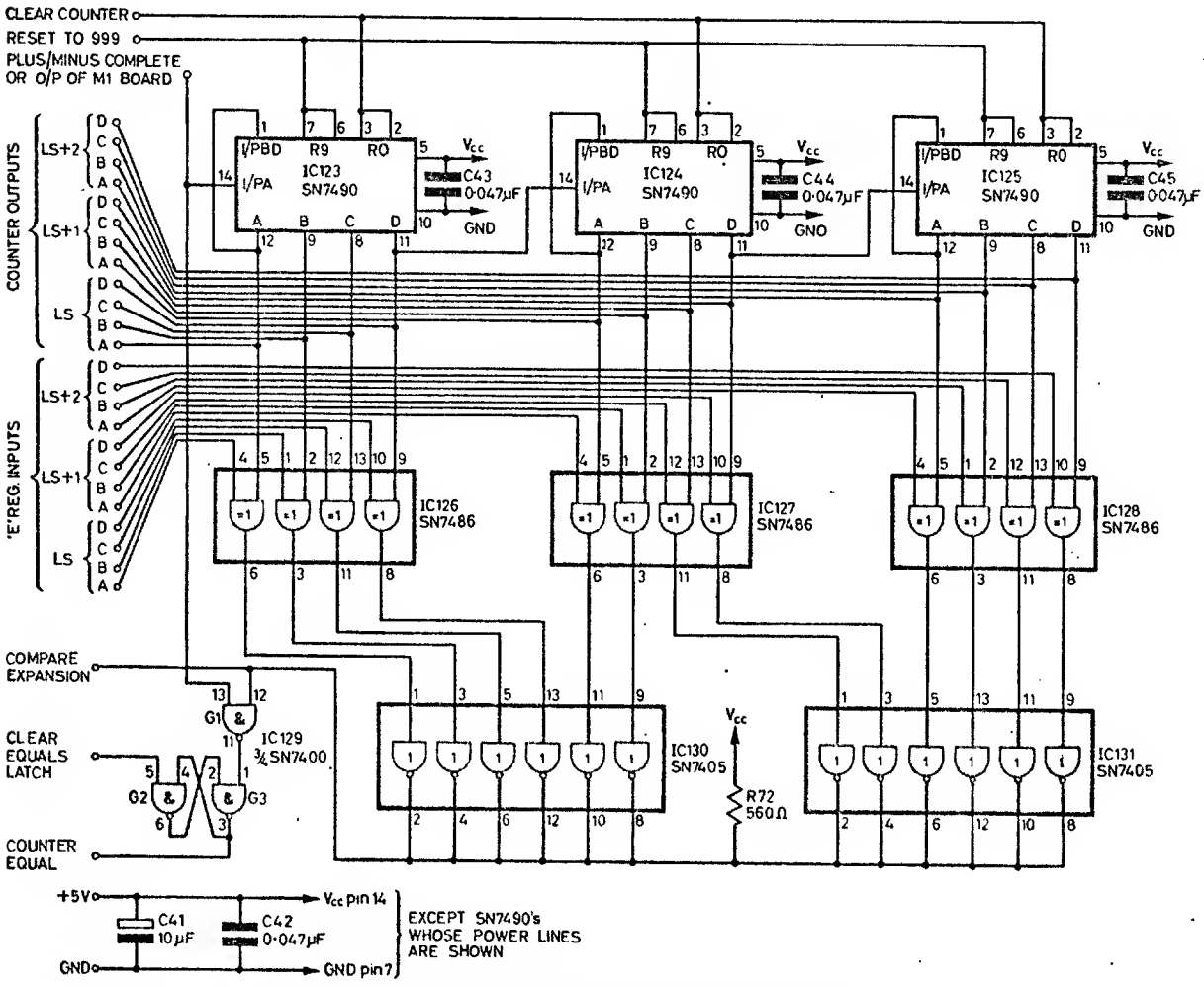


Fig. 10.3. Circuit diagram of one of the M boards. The other board is identical to this, both being built on DL109/44 boards

The count input to the board comes either from the PLUS/MINUS COMPLETE line (in the case of M1) or from the LS+2, D output of board M1 (in the case of M2).

Each of the SN7490 devices has a decoupling capacitor connected between its power supply lines, in addition to the two standard board decoupling capacitors C41 and C42.

LINE DRIVING

Special precautions are necessary for absolute integrity of the count, without false triggering or commutation, because the ABCD counter outputs are taken off the board as inputs to the A REGISTER.

Line driving from counters in this way can cause problems due to the high peak current required to charge the stray capacitance of the line during a 0 to 1 transition. Having an extra reservoir of charge available directly across the i.c. power pins goes a long way toward preventing the mistriggering problems which could result.

COUNTER PRESETS

The RESET 0 (R0) and RESET 9 (R9) inputs to the SN7490 set the COUNTER outputs to 0000 or 1001 respectvely.

The R0 inputs are connected together to form the CLEAR COUNTER line, controlled by the PROGRAMME, and the R9 inputs together make up the RESET to 999 line.

As mentioned in Part 1, it is necessary to preset the M COUNTER to 999999 before a division so that the final number of subtractions counted when the A REGISTER contents go negative and stop clock generation, is not the full number of subtractions performed, but the full number minus one.

Setting the count to 999999 is the same as starting to count from minus one, since on the first PLUS/MINUS COMPLETE pulse, the count will change to 000000, the number registered by the counter always being one behind the true number of subtractions performed.

During MULTIPLICATION the true number of additions performed has to be counted—the PROGRAMME ensuring this by energising the CLEAR COUNTER input and not the RESET to 999 input.

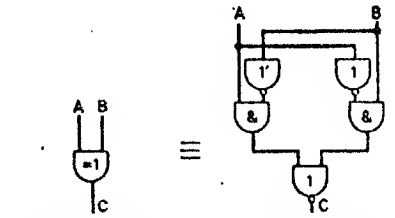


Fig. 10.4. Equivalent logic for an EXCLUSIVE-OR gate and truth tables for both positive and negative logic conventions

COMPONENTS

Resistors

R72, R73 560Ω ¼W ±10% (2 off)

Capacitors

C41, C46 10μF 15V elect. (2 off)

C42–45, C47–50 0·047μF (8 off)

Integrated Circuits

IC123–125, IC132–134	SN7490 (6 off)
IC126–128, IC135–137	SN7486 (6 off)
IC129, IC138	SN7400 (2 off)
IC130, IC131, IC139, IC140	SN7405 (4 off)

Printed Circuit Boards

Type DL109/44 Shirehall (2 off)

In each case components are divided equally between the two M boards

COMPARATOR

The COUNTER as described is all that is needed to allow the DIVISION operation to take place, but during MULTIPLICATION comparison of the count with the E REGISTER contents is required.

The COMPARATOR is made up of the remaining i.c.s on each board and is concerned solely with detecting the equality of E REGISTER and COUNTER outputs so that a control signal can be produced to stop the clock at this point.

The 24 bits of E REGISTER data and the 24 bits of COUNTER data are individually compared on a one-to-one basis in a series of 24 EXCLUSIVE-OR gates formed from six SN7486 packages, housed three to a board.

EQUIVALENCE GATE

The SN7486 package is a member of the M.S.I. family and is described as a quad EXCLUSIVE-OR gate in TTL literature. The very useful EXCLUSIVE-OR function has its own logic symbol, but is in fact made up of a series of simpler gates, as has its own logic symbol, but is in fact made up of a series of simpler gates, as shown in Fig. 10.4.

Readers may recognise the equivalent logic as being simply the common AND-OR-INVERT function together with a couple of inverters to produce the NOT version of the A and B inputs.

The reason for the EXCLUSIVE-OR name becomes obvious when the basic (positive logic) truth table is examined. The output from the gate is a logic 1 if either input A OR input B is a logical 1 but *not* if both are logical 1's.

This response is that of a non-equivalence gate since a logic 1 output is produced only when the inputs are different, but the situation is changed when the gate is examined in operation as a negative logic system, as the second truth table demonstrates.

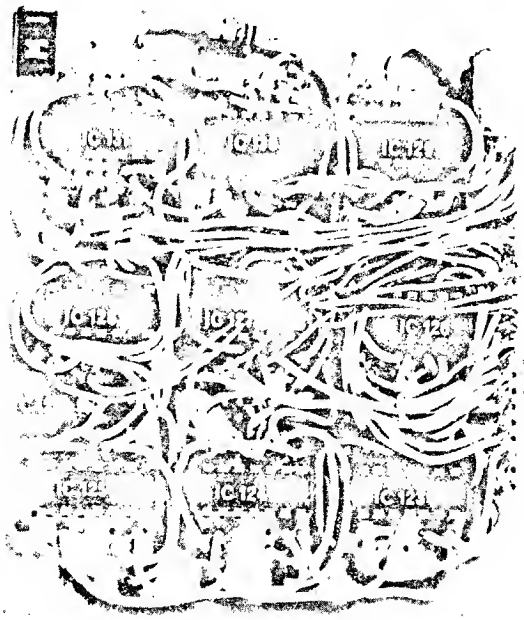
NEGATIVE LOGIC

In the second truth table we can see that when a low voltage is interpreted as a logic 1, rather than as a logic 0, the output of an SN7486 gate is a logic 1 when the inputs are identical, giving the equivalence function.

M COUNTER BOARDS

M1

M2/1	1	23	A2/35
not used	2	24	A2/36
not used	3	25	A1/35
not used	4	26	A1/36
E2/35, M2/22	5	27	A2/37
E2/36	6	28	A2/38
E2/37	7	29	A1/37
E2/38	8	30	A1/38
E1/29	9	31	A2/39
E1/30	10	32	A2/40
E1/31	11	33	GND
E1/32	12	34	+5V
E1/35	13	35	A1/39
E1/36	14	38	A1/40
E1/37	15	37	not used
E1/38	16	38	not used
CB/31	17	39	not used
not used	18	40	not used
CL LATCH (fr prog)	19	41	not used
CL CNTR (fr prog)	20	42	not used
RESET to 999 (fr prog)	21	43	not used
CB/41	22	44	not used

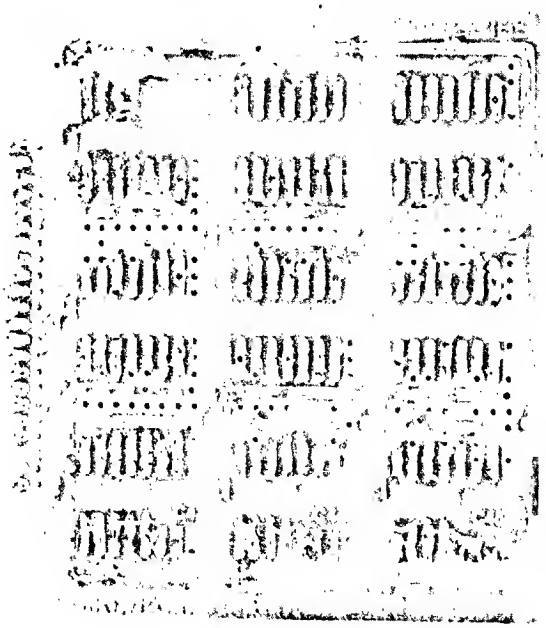


1	COMPARE EXPANSION	
2	not used	
3	not used	
4	not used	
5	D	E REG INPUTS
6	C	LS + 2
7	B	LS + 2
8	A	LS + 2
9	D	LS + 1
10	C	LS + 1
11	B	LS + 1
12	A	LS + 1
13	D	LS
14	C	LS
15	B	LS
16	A	LS
17	COUNTER EQUAL	
18	not used	
19	CL EQUALS LATCH	
20	CL CNTR	
21	RESET to 999	
22	COUNT INPUT	

Layout of components on upper side of M COUNTER board, and interconnection details of the M1 edge connector. See Fig. 6.9 for disposition of edge connectors

M2

CNTR OUTPUTS	LS + 2	D	23
		C	24
		B	25
		A	26
	LS + 1	D	27
		C	28
		B	29
		A	30
	LS	D	31
		C	32
		GND	33
		+5V	34
	LS	B	35
		A	36
	not used		37
	not used		38
	not used		39
	not used		40
	not used		41
	not used		42
	not used		43
	not used		44



M1/1	1	23	A2/27
not used	2	24	A2/28
not used	3	25	A1/27
not used	4	26	A1/28
E3/29	5	27	A2/29
E3/30	6	28	A2/30
E3/31	7	29	A1/29
E3/32	8	30	A1/30
E3/35	9	31	A2/31
E3/36	10	32	A2/32
E3/37	11	33	GND
E3/38	12	34	+5V
E2/29	13	35	A1/31
E2/30	14	36	A1/32
E2/31	15	37	not usod
E2/32	16	38	not used
not used	17	39	not used
not used	18	40	not used
not used	19	41	not used
CL CNTR (fr prog)	20	42	not used
RESET to 999 (fr prog)	21	43	not used
M1/5	22	44	not used

Layout of capacitors on underside (ignore unmarked capacitor) and interwiring details of M2 socket

To disbelievers, all this talk of switching logic conventions to suit the circumstances can be confusing, and really it is only a convenient way of looking at things.

In practical terms, the output of an SN7486 gate will go low when its inputs are identical, so to determine when all 24 gates have low outputs, i.e. when M equals E, we need a 24 input NAND gate which responds to negative logic inputs.

NEGATIVE LOGIC NAND GATE

No such gate is available in the standard TTL range, but if it were, it would be listed as a NOR gate because TTL is described in the positive logic convention.

All is not lost however since by using an open-collector inverter connected in the input of each SN7486, and then joining all the open collectors through a single common resistor to V_{CC}, i.e. by performing the WIRED-OR function at their outputs, a negative logic NAND gate of virtually unlimited size can be formed (Fig. 10.5).

The way a gate operates is fairly straightforward: if all SN7486 outputs are low, i.e. if M equals E, then the output of all inverters will be high, and the common resistor ensures a high voltage output.

If any one or more of the SN7486 outputs is high, however, one or more of the inverter outputs will go low and pull the common output to a low level.

INVERTERS

The inverters used on the M boards are type SN7405, which have the required open collector output circuitry. Note that the SN7404 devices are not suitable for use in this position due to their standard totem-pole outputs.

Although only one "pull-up" resistor is required for the full 24 inverters, electrically speaking in fact a separate resistor is used on each board to allow the boards to operate autonomously when required.

The inverter outputs from the two boards are united by means of the COMPARE EXPANSION input/output line, so that the two resistors are effectively in parallel.

LATCH FUNCTION

When an equality is registered by the comparator, the common output line rises to a high level and this signal is used to set the simple latch flip-flop made from cross-coupled SN7400 gates G2 and G3.

Setting the latch is carried out via another gate G1, which is controlled by the clock input line to

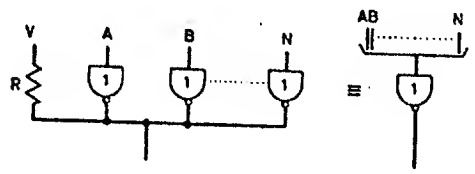


Fig. 10.5. The use of inverters to form a 24 input NOR gate

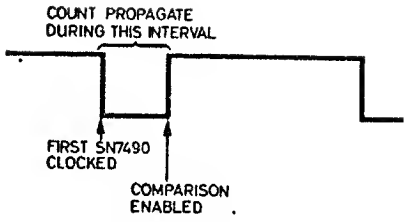


Fig. 10.6. PLUS/MINUS COMPLETE waveform from the COUNTER board

the first SN7490. In practice this line will carry the PLUS/MINUS COMPLETE waveform, since only the latch on the M1 board is wired into circuit.

The reason for this gated latch input circuit is explained in Fig. 10.6, which shows the PLUS/MINUS COMPLETE waveform from the COUNTER board.

The SN7490 counters are triggered from the negative going signal, but because these devices operate in the ripple count mode, there will be a significant count propagation delay time down the chain which can and will lead to transient spurious outputs from the COMPARATOR gating.

Using the PLUS/MINUS COMPLETE signal to gate the COMPARATOR output prevents the spurious outputs from setting the EQUALS LATCH until count propagation is complete, since G1 is enabled by the positive going edge of the waveform.

EQUALITY

When a genuine state of equality exists between the COUNTER and E REGISTER the latch is set, energising the COUNTER EQUAL line which in turn stops the supply of clock pulses to the A, Z and ADDER boards.

Before a further MULTIPLICATION sequence is initiated, the PROGRAMME clears the EQUALS LATCH ready for a new comparison.

CONSTRUCTION

Construction of the two M boards follows the by now familiar pattern, two DL109/44 cards being used. All wiring should be kept as short as possible whilst avoiding "bird's nests".

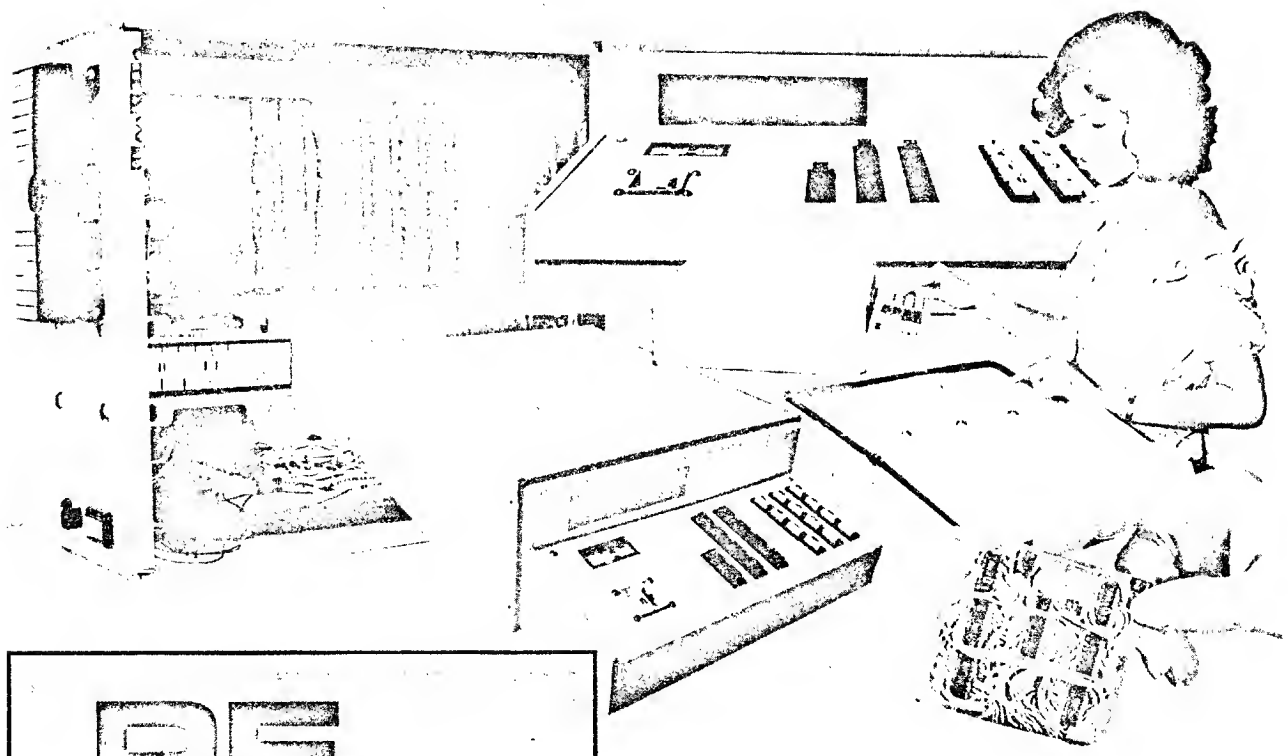
Speed problems decrease by a factor of ten for each stage of the COUNTER meaning in effect that only the first stage could be a problem in this respect. For this reason it is best to select which board is to be installed in the M1 position during test calculations, since the first stage of one board might perform better than the other at speed.

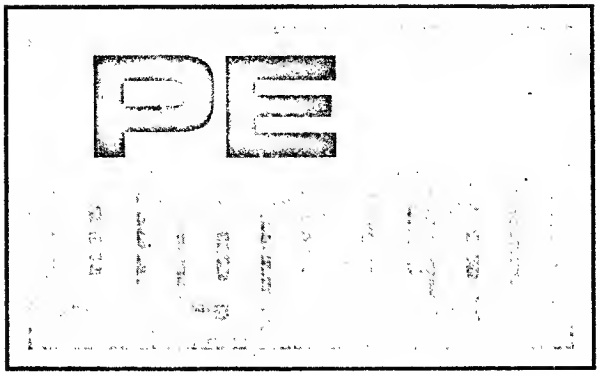
TESTING

The M boards are easy to check in isolation if required, but if the recommended sequence of construction has been followed and the calculator is operational on ADD/SUBTRACT, it is easier to test the boards in situ, using the MULTIPLY/DIVIDE programmes—but more of this next month.

Next month: E³ Logic, Error Detection and Testing

CONCLUDING ARTICLE





By R.W.COLES

PART 11

OVERFLOW LOGIC AND OVF BOARD

THIS final part of the Digi-Cal series describes the remaining logic housed on the under-chassis overflow (OVF) board, and attempts to knit together the loose ends which have been left dangling in earlier articles. Testing and troubleshooting information is also given.

OVERFLOW (OVF) BOARD

The existence of the OVERFLOW board was established in Part 2, when it was mentioned that this board is mounted copper side uppermost under the chassis, spaced from it by two 6BA nuts on each of the supporting bolts.

The OVF identity was not given to this board in Part 2 but is used here for ease of reference, the majority of the logic housed on this board being concerned with the OVERFLOW circuitry.

The Veroboard panel itself is mounted in the copper up fashion to facilitate the use of this board as an interconnection and power bus medium in addition to its job of housing logic. This mounting method also permits the easy addition of circuitry without access to the underside of the board, the only compromise necessary being that of neatness, since the solder is "on display" together with the components.

INTERCONNECTIONS

The OVF board carries the +5V and ground line power buses, from which the other logic cards are supplied. Any other logic lines which are employed, e.g. the FUNCTION CODE A and B are also allocated a copper strip for bus use to permit a tapping to be made where required.

Programme functions are distributed from the OVF board by means of a series of terminal pins which act as distribution points, the decision as to which functions require this treatment being left to the individual constructor as layouts will undoubtedly vary.

OVERFLOW LOGIC

The OVERFLOW logic is required to detect and indicate any errors resulting from the incorrect operation of the calculator, indication being provided via the red OVF lamp on the keyboard. If this lamp comes on at all during a calculation then an improper operation has been attempted and the only course open is to depress the CLEAR key which also resets the OVF circuits.

There are several ways in which an error condition can occur, an error being a state which would result in an incorrect answer being given. Detection of these states requires a combination of three separate logic groups whose areas of responsibility are as follows:

(a) ENTRY OVERFLOW. If too many digits are entered into the E REGISTER, the most significant data can be destroyed by being shifted out of the end of the register. This condition must be detected.
(b) A REGISTER OVERFLOW. If during a multiplication sequence, the product exceeds the capacity of the A REGISTER then the CARRY STORE will stay set at the end of an addition which is an indication of OVERFLOW.
(c) ANSWER OVERFLOW. The Digi-Cal A REGISTER has a ten digit capacity although only eight digits are displayed, the other two positions in the register being for transient use during programme execution. Should either of these two positions contain other than zeros at the end of a programme sequence then an OVERFLOW has occurred.

This type of OVERFLOW can occur during ADDITION, MULTIPLICATION and when a negative answer is produced in complement form.

OVF CIRCUITS

The active circuitry of the OVF board is shown in Fig. 11.1, where it can be seen that in addition to the OVF logic proper, IC141 and IC146 perform the functions of constant store buffering and E^2 gating respectively.

Bistable BS2 of IC144 acts as the common OVF latch, which is set by an output from any of the three separate OVERFLOW detection circuits, and which controls the OVF lamp driver on the KEYBOARD logic board. The OVF latch is cleared when the CLEAR key is depressed in response to an OVF indication.

The NOR section of IC145 which is a four-wide two-input AND-OR-INVERT gate combines the inputs from three detection circuits to drive the BS2 PRESET input, an output from any of the three resulting in a SET LATCH signal.

ENTRY OVERFLOW LOGIC

IC142 and G1 of IC143 are used to detect E REGISTER overflows. The system used here to monitor the B.C.D. outputs of the most significant digit position of the register with IC142, which, in this application, can be considered as a four-input positive NOR gate with a common disable input.

The output of IC142 is gated with the E CLOCK to generate the OVF output when necessary.

Gate IC142 is in fact waiting for one or more of its inputs to go to a logic 1, indicating that the most significant digit of the E REGISTER contains other than decimal zero.

On the arrival of a further clock pulse an error output is generated to set the latch.

A problem arises here since by using the straightforward E CLOCK an error output would be produced one step too early. What is really needed is an E CLOCK "pre-pulse" which comes and goes before the register itself is clocked. At first sight this is an impossible requirement to meet; however, by using the inherent propagation delays of the gates involved, such an arrangement can be achieved.

What happens is that when a B.C.D. output other than zero appears in the most significant position of the register a 1 input to pin 9 of IC145 results.

Much later, when another number key is pressed the rising E CLOCK on IC145, pin 10 will result in an error output to pin 8, setting the latch. Even before the clock rises on pin 10, the unbuffered E CLOCK operates the common disable input connected to pins 1, 3, 5 and 9 of IC142 removing the 1 input to IC145, pin 9.

The result at the output of IC145 is an extremely narrow pulse which in practice could be too narrow to set the latch BS2. The way to stretch this pulse is to increase the propagation delay through IC142 and G1 of IC143, and this can be conveniently achieved by increasing the capacitive load on the output of IC142.

A capacitor C_x is shown on the diagram and can be added if the error output is found to be too short on test; the value used should be between 200pF and 1,000pF.

No such capacitor was necessary on the prototype.

A REGISTER OVERFLOW LOGIC

The operation of the A REGISTER detection logic is quite straightforward; in this case the task is simply to detect the presence of a stored carry at the end of ten clock pulses during a multiplication or addition.

The rising edge of the END OF TEN output from board CB triggers a monostable made up of BS1 of IC144 and G2 of IC143. The indication that the clock sequence is at an end is gated with the CARRY SENSE output from board AD, in G3.

The output of G3 is gated with an inverted FUNCTION CODE A (which is an indication of the arithmetic operation being performed) in the AND section of IC145 to produce the ERROR output at pin 8.

ANSWER OVERFLOW LOGIC

Detecting an integer in the two most significant A REGISTER positions seems on the face of it to be quite straightforward, but in practice such considerations as lack of space on the A boards to install i.c. gates, and lack of edge contacts on the A boards to allow external i.c. gates pose some problems.

The only practical solution is to construct a special gate using discrete components which operates as a positive logic NOR. This design requires only the installation of four diodes, and the utilisation of only one edge contact on each A board.

The problem of the low logic 1 levels associated with TTL outputs is overcome by clamping the emitter of TR22 of the gate to about $\frac{1}{2}V_{cc}$, and using TR23 to regenerate suitable logic levels to interface with IC145 pin 13.

Pin 1 of IC145 gates the ERROR output from the discrete component gate with what is effectively an END OF PROGRAMME signal (DISPLAY A) so that valid transient outputs from TR23 during programme execution have no effect on the OVF LATCH.

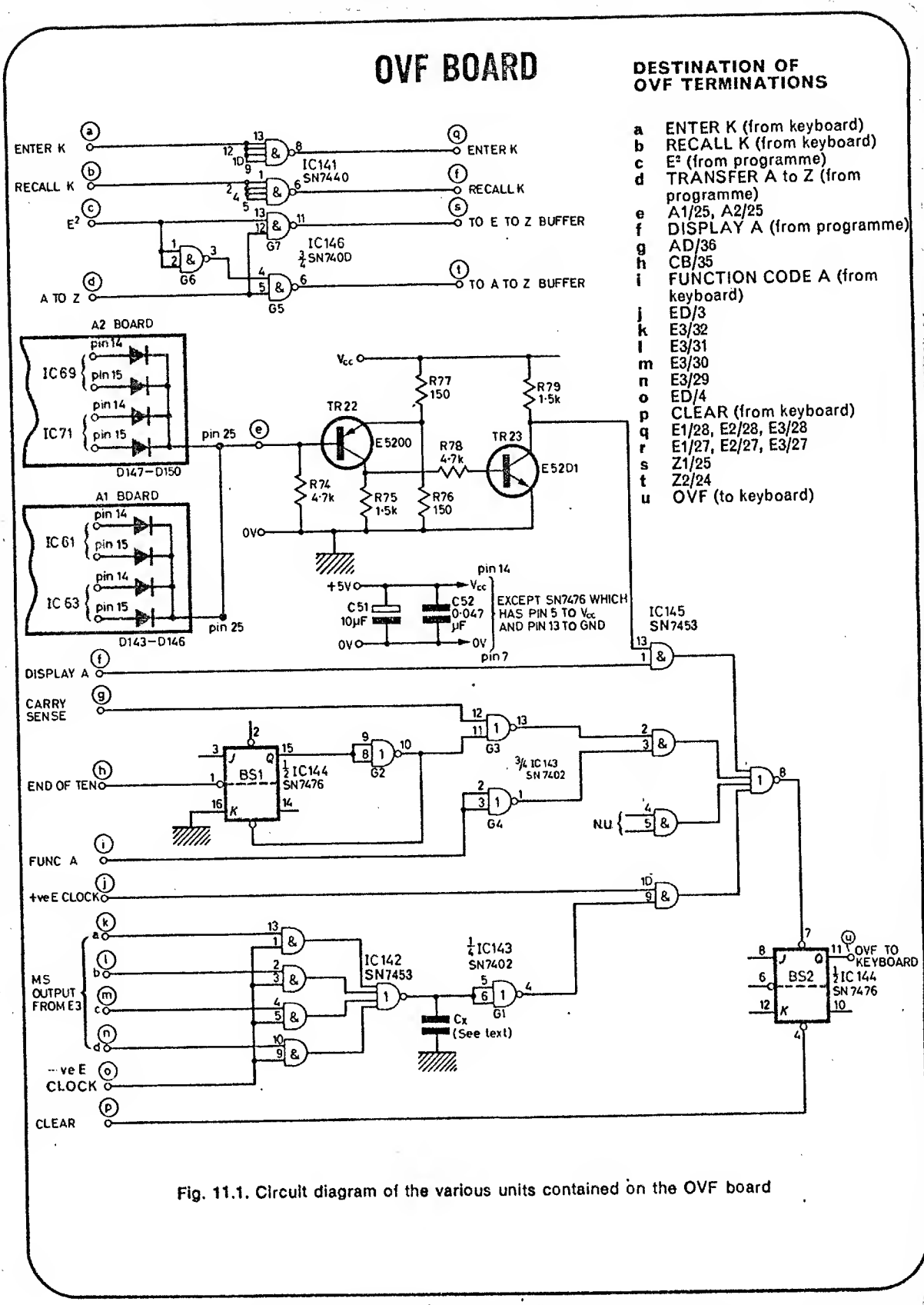


Fig. 11.1. Circuit diagram of the various units contained on the OVF board

DIVIDE OVERFLOW

No logic has been included to show that an OVERFLOW during a DIVISION operation has occurred.

Logic to fulfil this function would be simple to design and could use pins 4 and 5 of IC145 as an access to the OVF LATCH, but this was not carried out on the prototype because a divide overflow is very obvious to the operator by virtue of the fact that no answer is produced on the display.

E SQUARED GATING

It was only after the component location stage of Digi-Cal design that it was realised that the addition of a very few gates could produce an automatic E^2 facility to complement the basic arithmetic functions.

The gating required is so simple that the incorporation on the OVF board is quite straightforward.

The object of the three gates shown in Fig. 11.1 as part of IC146 is to divert the A to Z transfer command from the PROGRAMME to the E to Z buffer gate when the E^2 latch on the PROGRAMME board is set.

This simple operation causes the MULTIPLY programme to multiply the number in the E REGISTER by itself. The normal command to transfer the A REGISTER contents to the Z REGISTER is blocked and the E to Z transfer substituted, resulting in the number E being both multiplier and multiplicand.

CONSTANT STORE BUFFERS

IC141 is an SN7440 buffer gate which is interposed between the KEYBOARD outputs and the constant store to provide the drive and inversion

OVF LOGIC CONSTRUCTION

Although the E^2 logic and the constant store buffers will have to be wired up before the testing stage, it is best to leave the OVF detection logic until the calculator is operating correctly. Connecting up these circuits before proper operation is realised could lead to confusion.

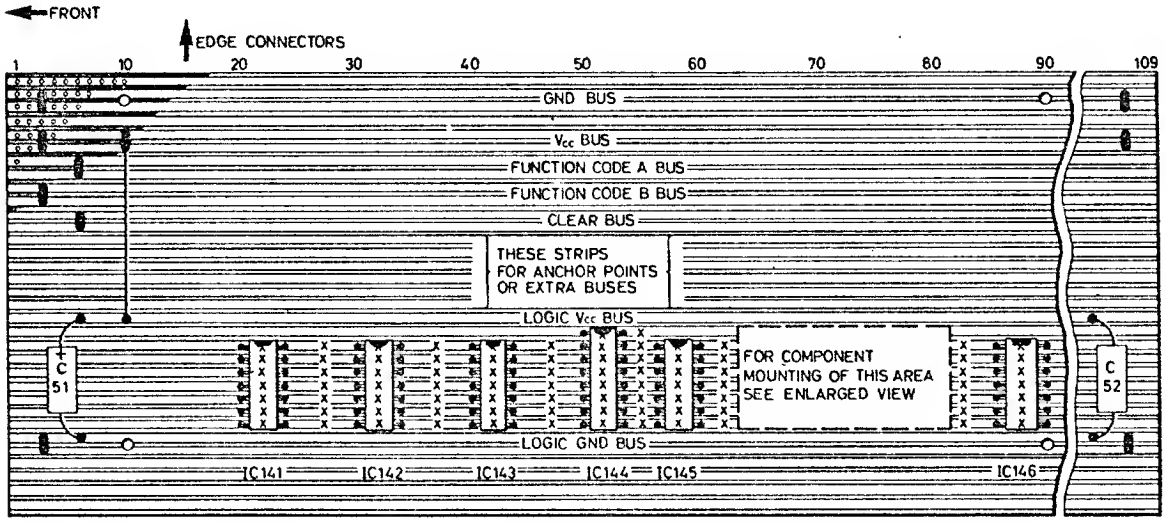
Having both the i.c.s and the wiring on the copper side of the board takes a little getting used to when soldering, but there are no special problems to look out for, and circuit tracing is really much easier. The board layout is shown in Fig. 11.2, and mounting position in Fig. 11.3.

OVERALL TESTING

It would be a very optimistic constructor indeed who wired up the whole Digi-Cal, switched on, and expected it to work perfectly first time.

There will no doubt be wiring errors, perhaps a faulty i.c. (there were three in the prototype), and a dry joint or two.

The policy of piecemeal testing suggested in previous parts will undoubtedly have eliminated most



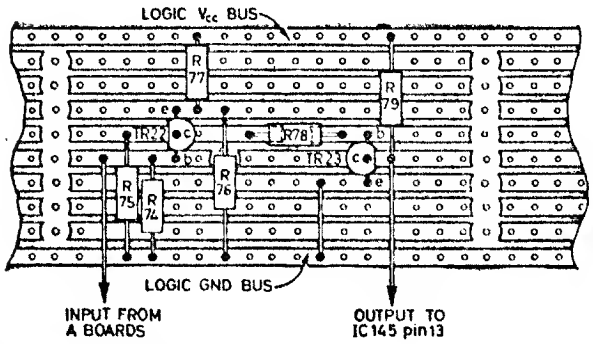


Fig. 11.2. Construction of the OVF board. Note that both the wiring and components are placed on the copper strip side of the Veroboard panel

COMPONENTS

OVF BOARD

Resistors
R74 4·7kΩ
R75 1·5kΩ
R76 150Ω
R77 150Ω
R78 4·7kΩ
R79 1·5kΩ

Capacitors
C51 10μF 15V elect.
C52 0·047μF
C_x (see text)

Diodes
D143–150 West Hyde type "red" or any small silicon diode (8 off)

Transistors
TR22 E5200 } (West Hyde)
TR23 E5201 }

Integrated Circuits
IC141 SN7440
IC142 SN7453
IC143 SN7402
IC144 SN7476
IC145 SN7453
IC146 SN7400

Miscellaneous
11in × 3·6in × 0·1in matrix Veroboard panel

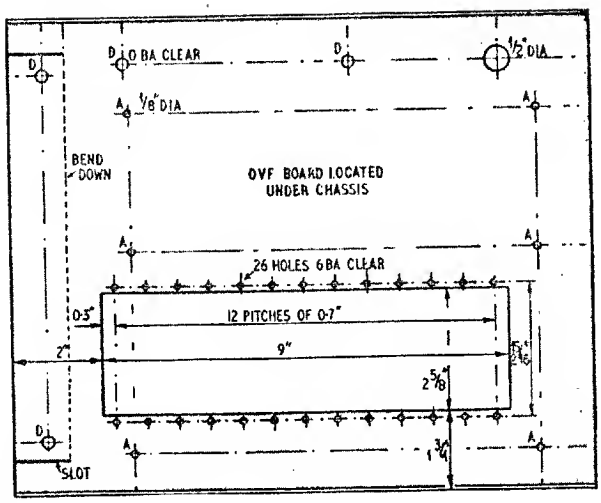


Fig. 11.3. The OVF board is mounted on the underside of the chassis in the four holes marked "A" in the main chassis plate

faults, and certainly the constructor who has reached the final testing stage, which basically involves making the programmes work as required, will be sure that all the boards are fundamentally serviceable.

The first hurdle to be cleared is the correct operation of the ADD/SUBTRACT programme and when this has been achieved (with a slow clock speed if desired) the bulk of the arithmetic section can be given a clean bill of health.

The MULTIPLY and DIVIDE programmes can then be tackeld in turn and if any problems are encountered a thorough understanding of the way the calculator should be operating will soon sort these out.

It cannot be stressed enough that after gathering evidence via a multimeter and display, the best strategy in solving a problem is to sit down with a paper and pencil and ponder the possible causes: aimless probing will get you nowhere.

CLOCK SPEED

The ultimate objective of the testing phase is to increase the clock speed to as high a rate as possible while maintaining correct operation.

In the prototype a speed of over 1MHz was obtained despite the far from ideal underchassis "bird's nest" wiring resulting from prototype modifications.

Constructors should be able to do better than this easily since all improvements have been incorporated in the published designs and any advance achieved in this respect will be rewarded by a shorter maximum multiplication time, important when operating near to the maximum capacity of the machine. ★

Corrections. We apologise for these errors which occurred during the course of Digi-Cal articles.

Part 3, Fig. 3.2. Capacitors C3, C4, C5 and C6 should be connected between +5V and GND, not as shown. The strobe outputs from IC7 are reversed, i.e. pin 12 should be strobe 8 and pin 4 should be strobe 1.

Part 4, Fig. 4.2. Switch S19 is shown twice, the K switch should be S5. S13 is shown twice, the **Decimal Point** switch should be S3. Both are shown correctly on Fig. 4.5. The diode labelled D103 on IC26 should be D101.

Part 5, Fig. 5.8. The K switch should be labelled **Recall K output.**

Part 6, Fig. 6.10. Connection from the Z1 and Z2 sockets to the E1, E2 and E3 boards show the pin numbers incorrectly. Correct destinations can be found by adding 22 to each of the pin numbers associated with the E boards, e.g. Z1/1 should go to E3/31. Also Z1/19 should go to AD/41, and Z1/20 to AD/42. Z2/19 goes to AD/39; Z2/20 to AD/40, not as shown. Z2/44 should go to Z1/42 and Z2/42.

A1/1 should go to AD/27; A1/10 to AD/31; A1/11 to AD/32.

A2/1 should go to AD/25; A2/10 to AD/29; A2/11 to AD/30.

Fig. 6.7. CP in IC77 and 78 should go to pin 3 not 2.